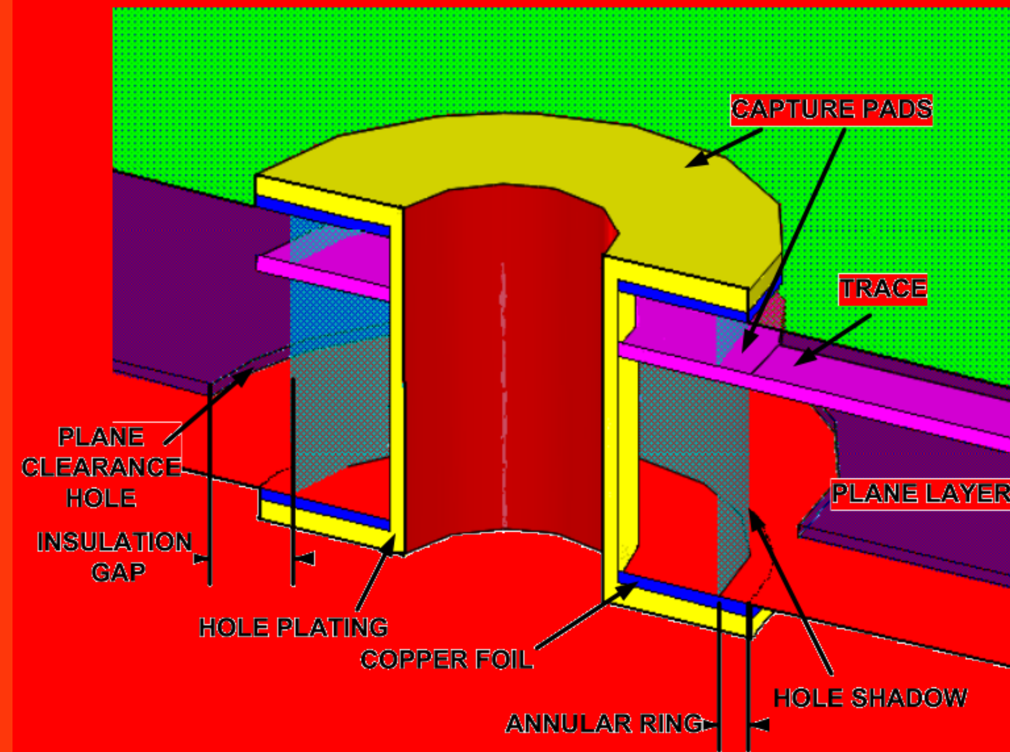


Universidad de Granada
Departamento de Electrónica y Tecnología de Computadores

Plated Through Hole Components

Padstack

Curso 15-16

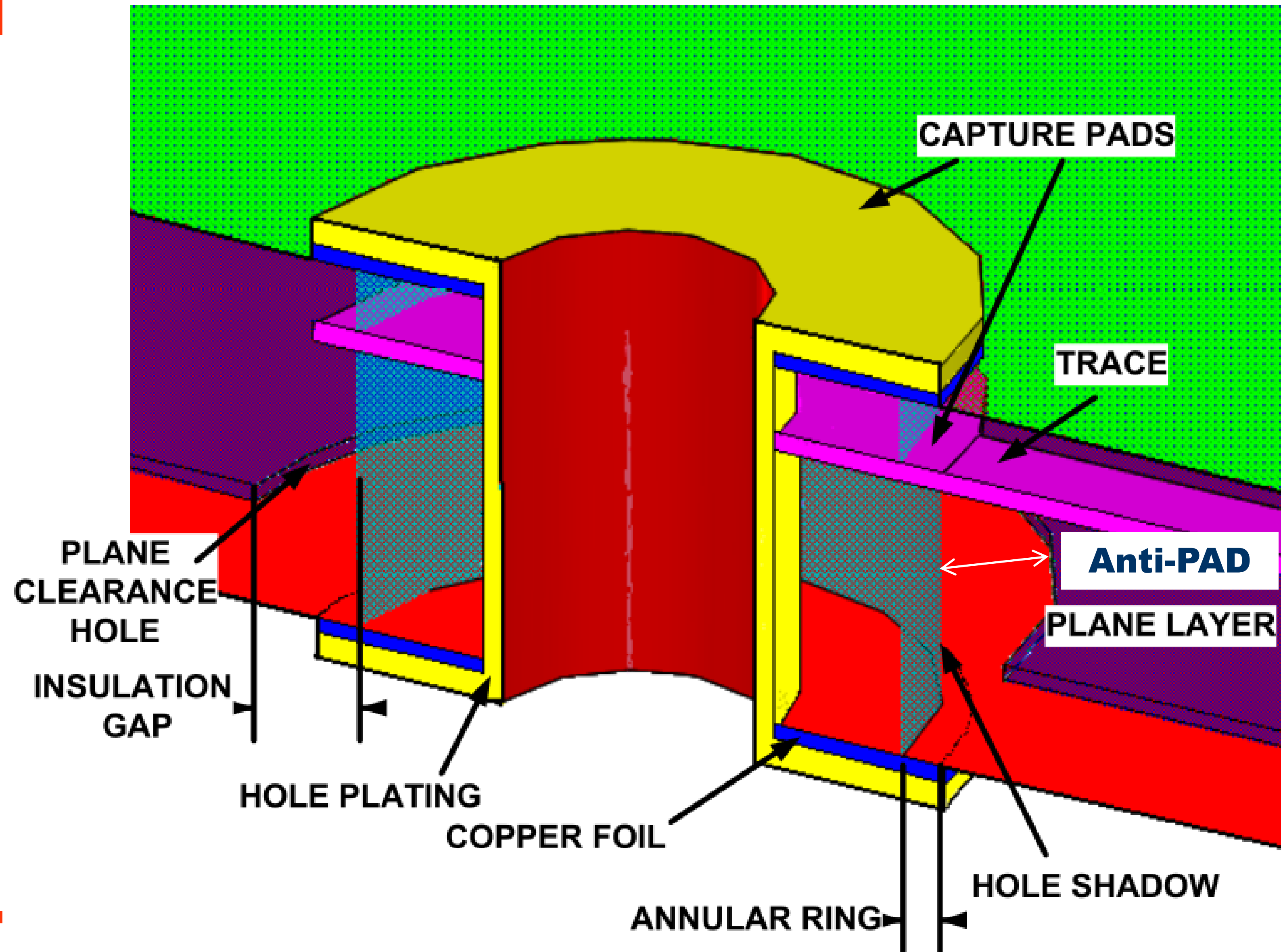
Prof. Andrés Roldán Aranda

4º Curso Grado en Ingeniería de Tecnologías de Telecomunicación

Contenidos

1.- Arquitectura del Pad
2.- Conceptos
3.- Tipología de Pads
4.- Surface Mount Technology
5.- Stencils
6.- Dimensionado de pistas

PAD Architecture



Conceptos

Finished hole size :the diameter of the plated through hole after all plating steps are completed.

Drilled hole size- the diameter of the hole after drilling.

Capture pad- the pads placed on outer layers to "capture" the plated through hole or on inner layers to connect traces to the plated through hole. Capture pads are used on inner layers only when a connection is being made to a trace. Putting capture pads on inner layers where no connections are being made are called nonfunctional pads and are not beneficial. Note: For mechanical mounting holes that are not plated, there is no need to place capture pads on the outer layers.

Clearance hole- the hole etched in a copper plane to allow a drilled hole to pass through. The hole may be plated or unplated.

Hole shadow- the shadow cast through all PCB layers by the drilled hole. Features in signal layers must be kept away from this "shadow" by a dimension corresponding to the insulation thickness required to meet appropriate standards. The hole shadow is defined by the diameter of the drilled hole and the worst case wander that the hole may have in the final PCB. This "wander" is composed of drilling inaccuracies, layer to layer registration
inaccuracies, inaccuracies in the working artwork and shrinkage of the laminate layers from the heat of lamination. Because of hole wander, plated copper may be found out to the edge of the hole shadow. Therefore, insulation thickness must start at the hole shadow and extend outward in both power and signal layers.

Manufacturing tolerance- the dimension that describes how a drilled hole will wander out of its true position. The inaccuracy components are described in the hole shadow description.

Hole plating- the copper plating deposited in a hole to create a connection between signal pins and traces or power pins and power planes. This plating is deposited after the PCB has been laminated and drilled.

Copper foil- the outer layers of all PCBs are formed using copper foil. This foil serves as an electrical path to conduct the plating current needed to plate copper in the holes and on the pads and traces that will be present on the surfaces of the finished PCB. After the plating steps have been completed, the foil is etched to form the traces, pads and other outer layer features.

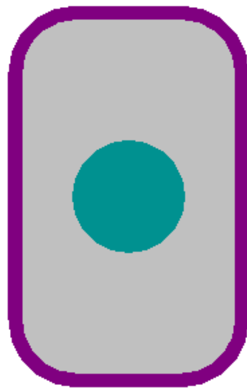
Conceptos

Insulation gap- the insulating material that exists between the hole shadow (copper plating in the hole) and metallic features in all of the layers. Examples are traces and planes.

Annular ring- the copper in the capture pad that extends past the drilled hole shadow. The capture pad is intentionally made larger than the drilled hole and the hole shadow in order to insure that there is always a portion of the pad making contact with the trace, even when the drilled hole is out of position due to drill tolerances.
Plane- any copper plane layer inside the PCB. Could be ground, Vdd or any other plane used to make electrical connections or to serve as partners for controlled impedance lines.

Pad Stack- the name given by CAD systems to describe the sizes of the capture pad, plane clearance, drill size and plating. The methods used to calculate these will be described in this document.

Tipos de PADs



Pad [mm]

1
YOUT_ALT

Top Layer | Bottom Layer | Top Paste | Bottom Paste | Top Solder | Bottom Solder | **Multi-Layer**

Location

X	93.7mm
Y	24.9mm
Rotation	0.000

Hole Information

Hole Size: 0.9mm

- (•) Round
- ( ) Square
- ( ) Slot

Properties

Designator	1
Layer	Multi-Layer
Net	YOUT_ALT
Electrical Type	Load

Plated [x] Locked [x]

Jumper ID: 0

Testpoint Settings

	Top	Bottom
Fabrication	[ ]	[x]
Assembly	[ ]	[ ]

Size and Shape

(•) Simple ( ) Top-Middle-Bottom ( ) Full Stack

X-Size	Y-Size	Shape	Corner Radius (%)
1.5mm	1.5mm	Rounded Rectang	50%

Edit Full Pad Layer Definition...

Offset From Hole Center (X/Y): 0mm 0mm

Paste Mask Expansion

- (•) Expansion value from rules
- ( ) Specify expansion value: 0mm

Solder Mask Expansions

- (•) Expansion value from rules
- ( ) Specify expansion value: 0.1mm

[ ] Force complete tenting on top

[ ] Force complete tenting on bottom

OK Cancel

Layer Stack Manager

Layer Stack Manager

TopLayer
MidLayer1
InternalPlane1 ((No Net))
InternalPlane2 ((No Net))
MidLayer2
BottomLayer

Total Height (71.4mil)
Core (12.6mil)
Prepreg (12.6mil)
Core (12.6mil)
Prepreg (12.6mil)
Core (12.6mil)

Layer Pairs
Top Dielectric
Bottom Dielectric
Add Layer
Add Plane
Move Up
Move Down
Delete
Properties ...
Configure Drill Pairs...
Impedance Calculation...
Place Stackup Legend

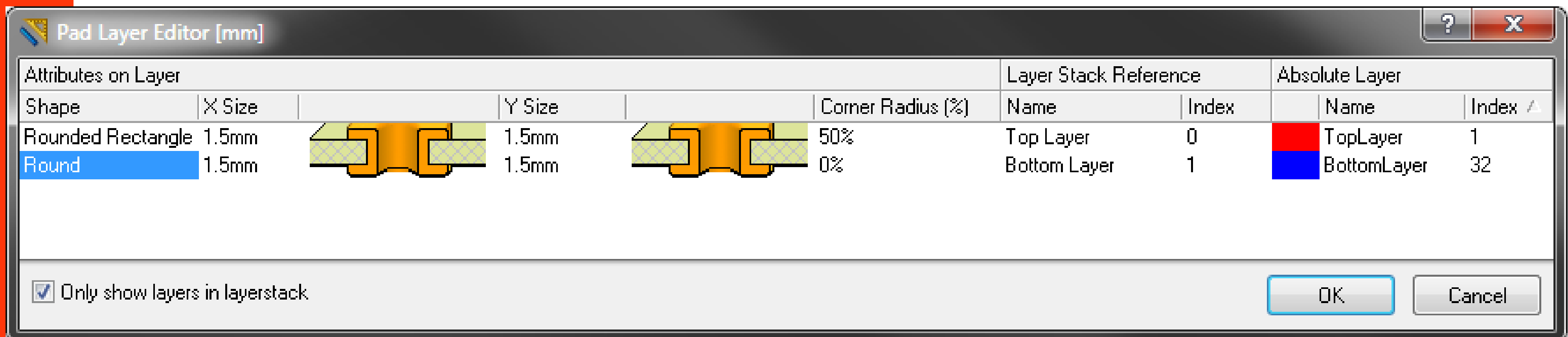
Menu
OK
Cancel

ugr Universidad de Granada
Departamento de Electrónica y Tecnología de Computadores

Tipos de PADs

Three layering options are available:

- **Simple** - specify a size and shape which is used for the pad on each affected layer in the pad stack.
- **Top-Middle-Bottom** - specify a different size and shape for the pad on the top, mid and bottom layers of the pad stack respectively.
- **Full Stack** - allows you to define the **pad size** and **shape** for each of the affected layers in the pad stack, on a layer-by-layer basis. Editing of the full pad stack is carried out in the Pad Layer Editor dialog, accessed by clicking the **Edit Full Pad Layer Definition** button:



ugr Universidad de Granada
Departamento de Electrónica y Tecnología de Computadores

Formas de PADs

Rounded Rectangle:

Pad [mm]

Top Layer | Bottom Layer | Multi-Layer

Location

X	169.24mm
Y	2.4mm
Rotation	0.000

Size and Shape

Simple | Top-Middle-Bottom | Full Stack

X-Size	Y-Size	Shape	Corner Radius (%)
1.5mm	1.5mm	Rounded Rectang	50%

Formas de PADs

Round:

Pad [mm]

Top Layer | Bottom Layer | Multi-Layer

Location

X	169.24mm
Y	2.4mm
Rotation	0.000

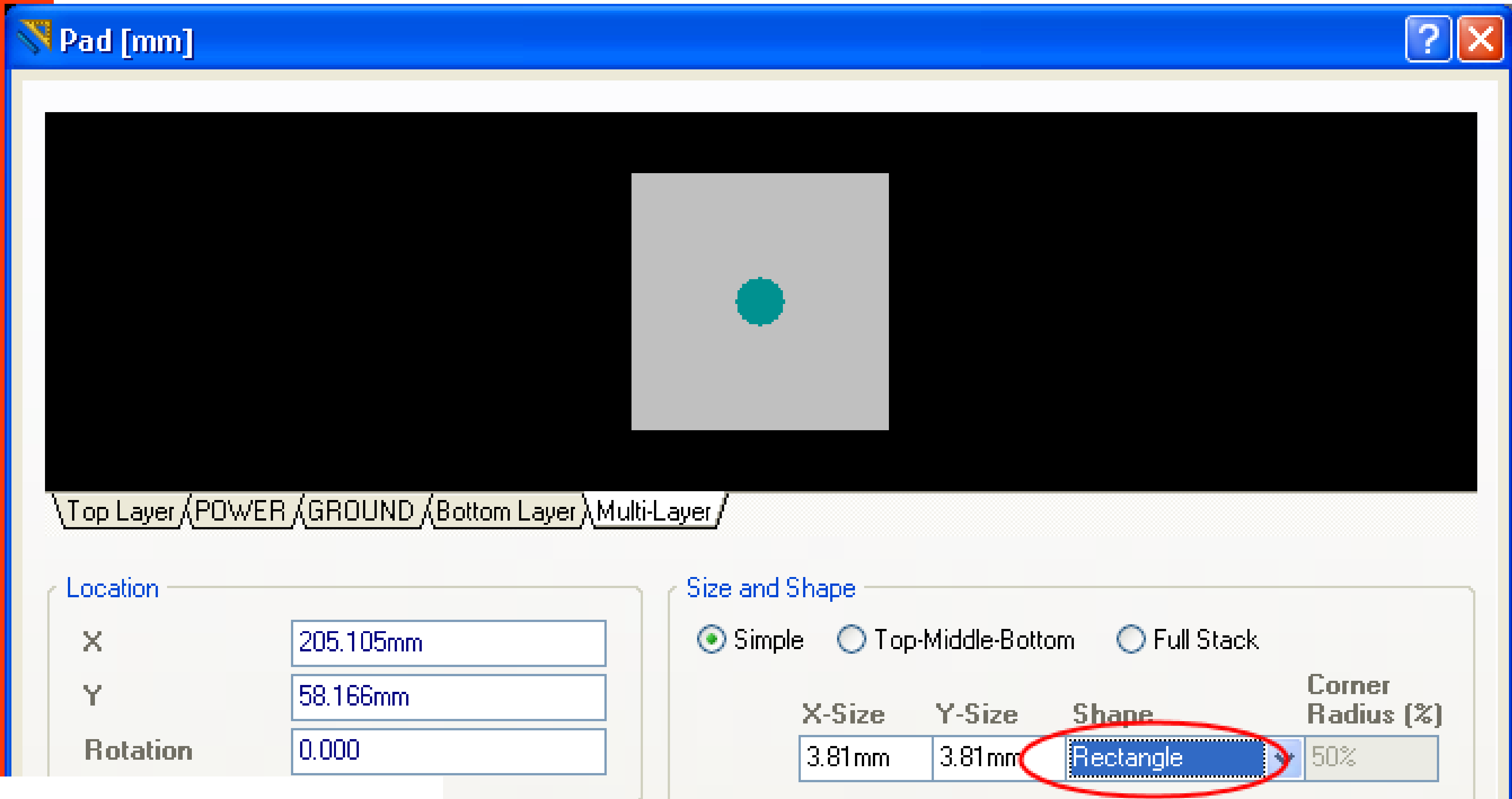
Size and Shape

Simple | Top-Middle-Bottom | Full Stack

X-Size	Y-Size	Shape	Corner Radius (%)
1.5mm	1.5mm	Round	50%

Formas de PADs

Rectangular:



Universidad de Granada
Departamento de Electrónica y Tecnología de Computadores

Formas de PADs

Octogonal:

Pad [mm]

Top Layer | POWER | GROUND | Bottom Layer | Multi-Layer

Location

X 205.105mm

Y 58.166mm

Rotation 0.000

Size and Shape

Simple | Top-Middle-Bottom | Full Stack

X-Size	Y-Size	Shape	Corner Radius (%)
3.81mm	3.81mm	Octagonal	50%

Thermal Relief (SPOKE)

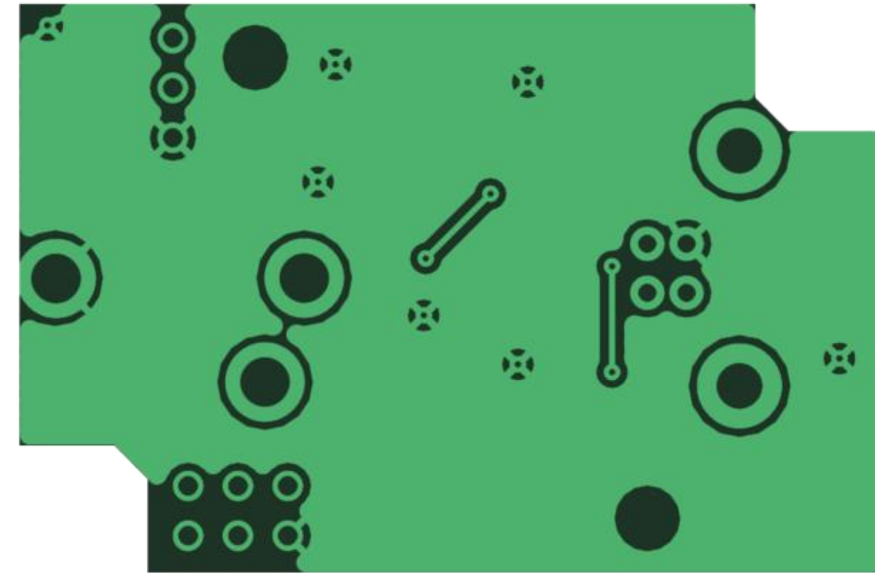
A **thermal relief** pad is a printed circuit board (PCB) pad connected to a copper pour using a thermal connection. It looks like a normal pad with copper "**spokes**" connecting it to the surrounding copper.

Radios de Bicicleta

A pad directly connected to the copper pour is difficult to solder since the heat quickly leaks away from the pad into the copper pour due to high thermal conductivity of copper.

A thermal connection restricts the heat flow, making the pad easier to solder.

Via holes that only connect one layer to another, without having soldering wires or pins into the hole, do normally not need thermal restriction.



Thermal Tie:

A = capture pad
B = clearance pad
C = tie width

A

Thermal Tie

C

Capture Pad

B

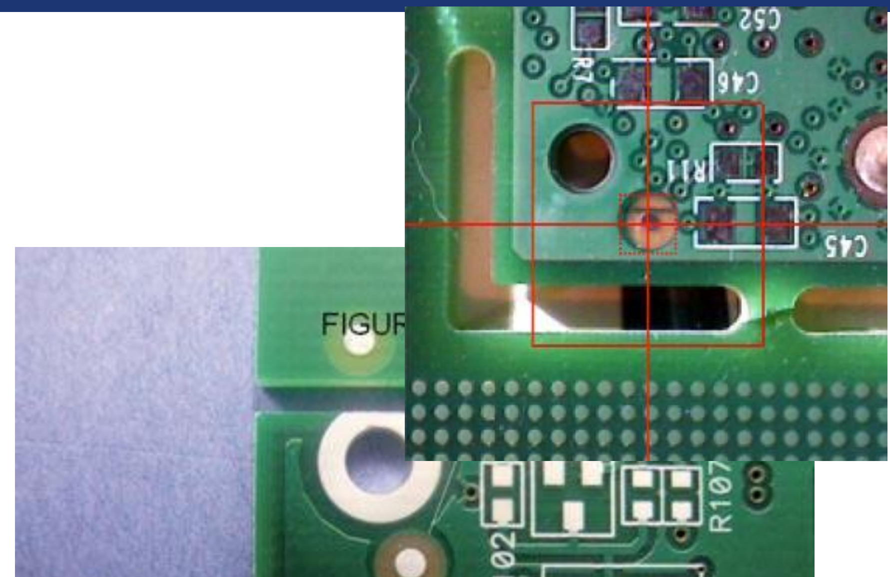
Thermal Isolation

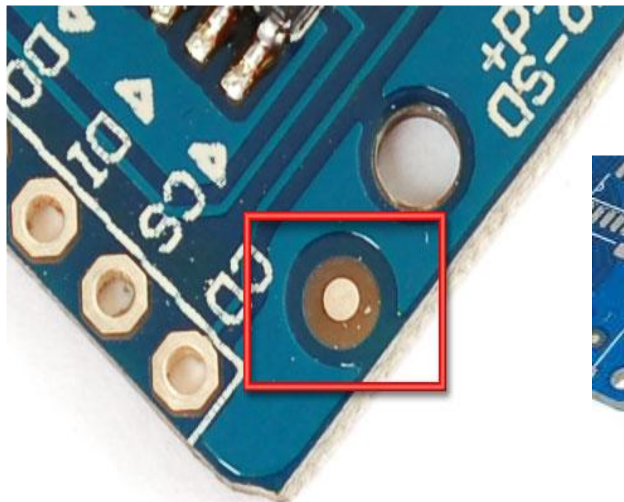
Basic Thermal Tie Geometry

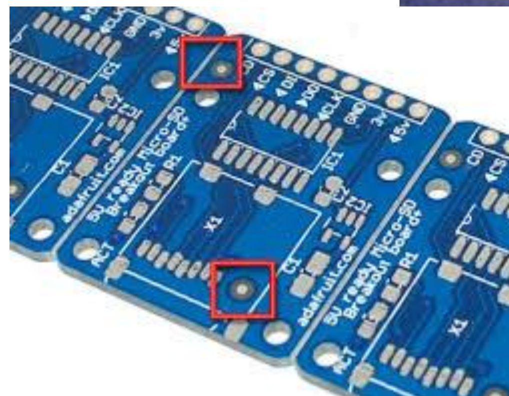
Fiducial Pad

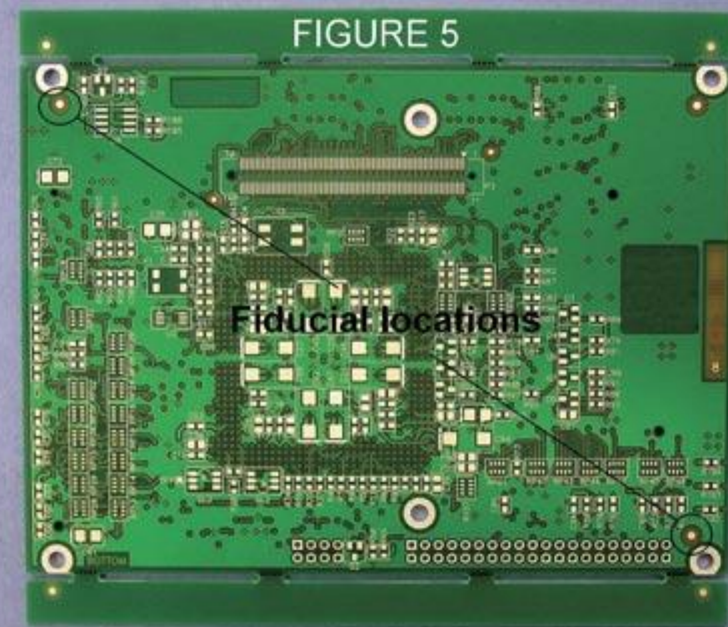
Fiducials are little target registration marks that are printed on PCBs, they are placed on the **top copper layer** (and bottom if you're doing 2-layers) and **allow the vision system** of the pick and place to recognize where the PCB is at.

They are **not placed on the mask or silk** because they are not as precisely aligned to the parts as the copper itself.







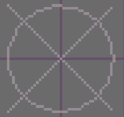


Departamento de Electrónica y Tecnología de Computadores

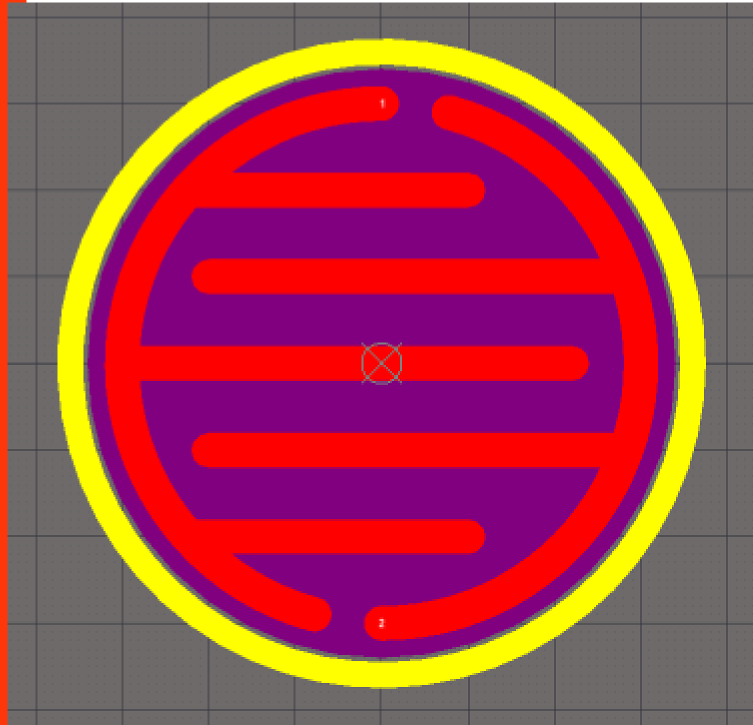
PADs Shapes

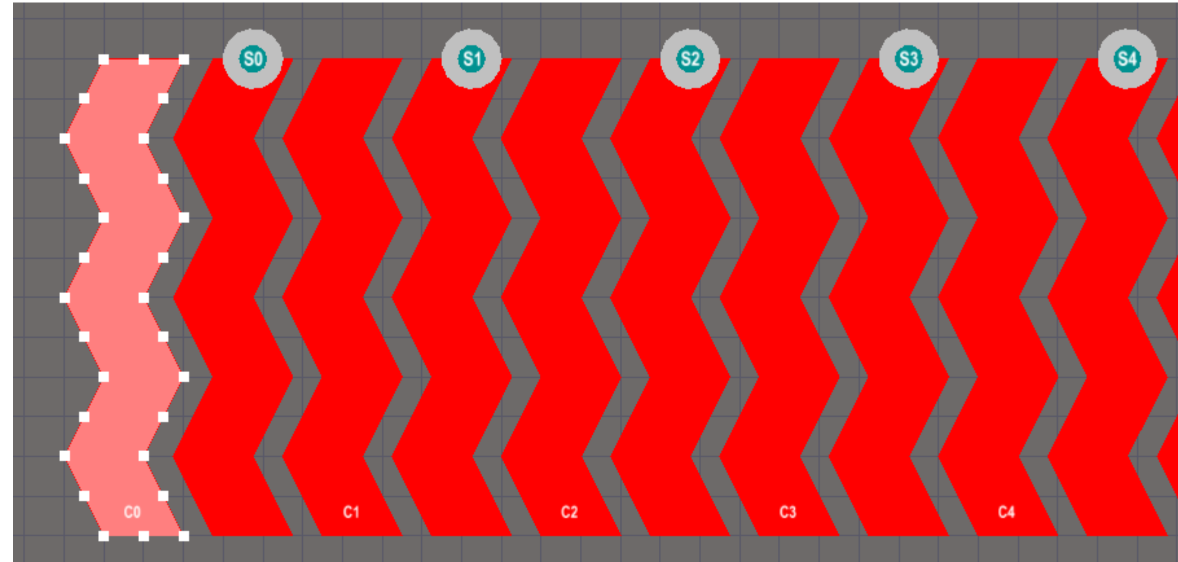
PADs Shapes

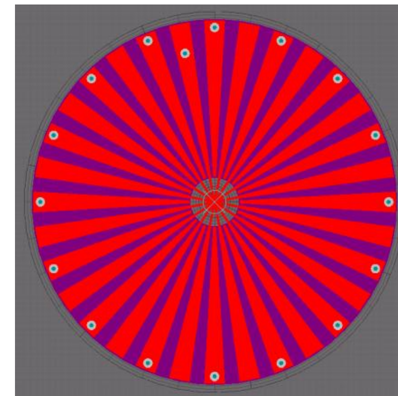
x: 4.250 dx: 0.000 mm
y: 1.450 dy: 0.100 mm
Snap: 0.05mm Hotspot Snap (All Layers): 0.2mm

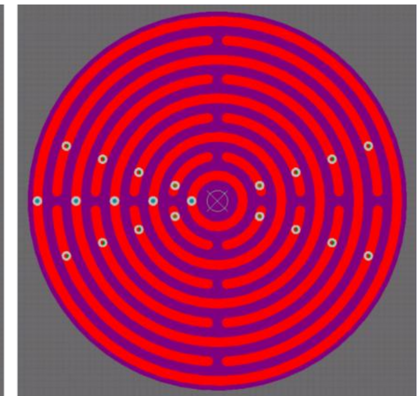


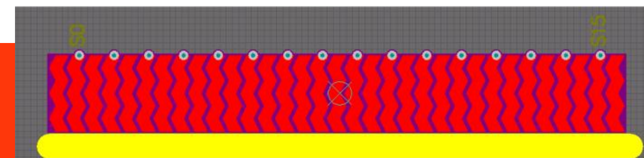
PADs Shapes

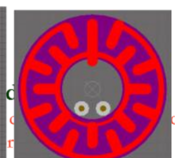




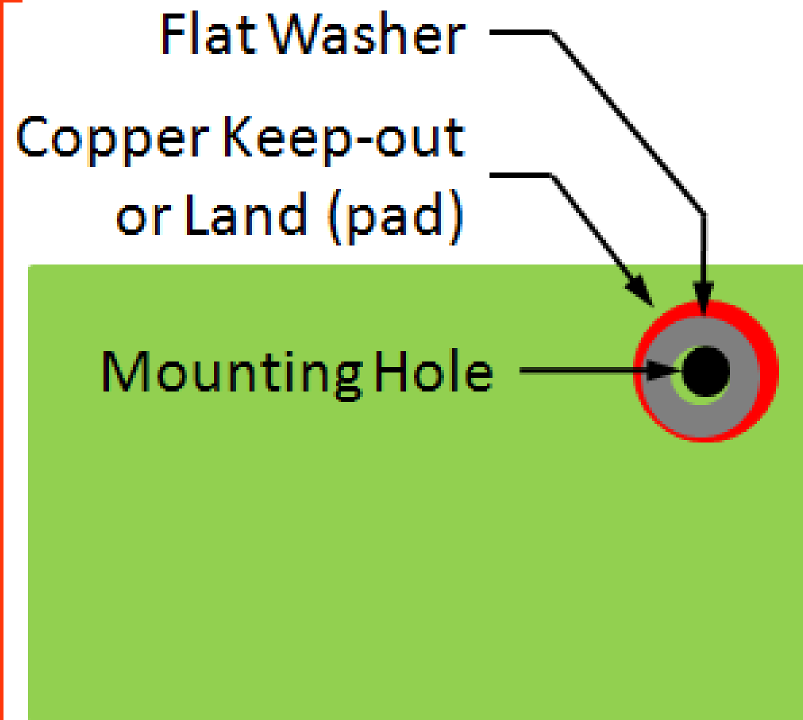








Mounting PADs:



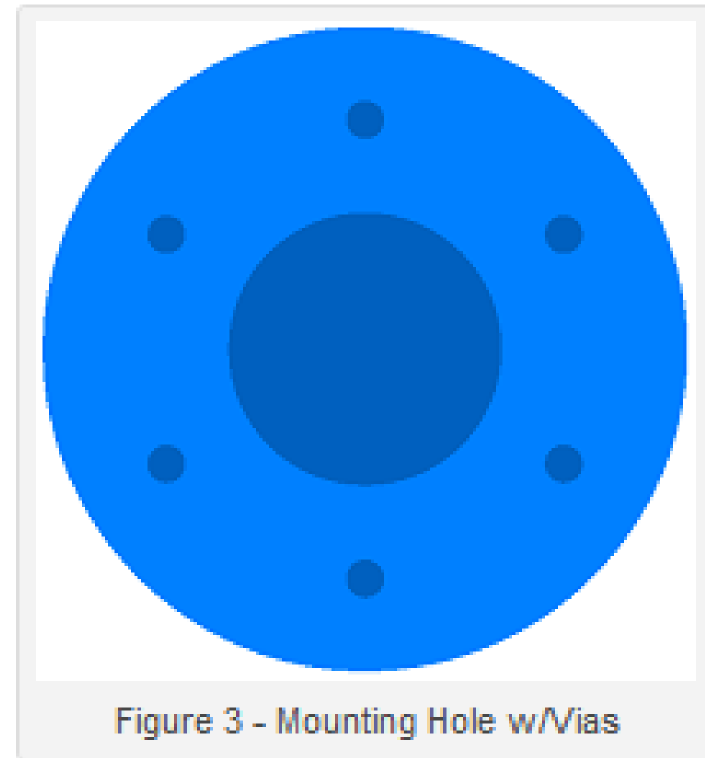


Figure 3 - Mounting Hole w/Vias

4 Layer Example

Package Solder Pad

0.18 mm
(square)

Component Traces

1.5748 mm

1.5038 – 1.5748 mm Component Trace

1.0142 – 1.0502 mm Ground Plane

Thermal Via

0.5246 – 0.5606 mm Power Plane

Thermal Isolation
(power plane only)

0.0 – 0.071 mm Board Base & Bottom Pad

Package solder pad (bottom trace)

Bibliography

FYI here's a Cirrus Logic app note ("Thermal Considerations for QFN Packaged Integrated Circuits")

http://www.cirrus.com/en/pubs/appNote/AN315REV1.pdf

Here's an Actel app note ("Assembly and PCB Layout Guidelines for QFN Packages")

http://www.actel.com/documents/QFN_AN.pdf

A Texas Instruments app note ("PowerPAD Thermally Enhanced Package"):

http://focus.ti.com/lit/an/slma002g/slma002g.pdf

And an Amkor app note: ("Application Notes for Surface Mount Assembly of Amkor's MicroLeadFrame (MLF) Packages")

http://www.amkor.com/index.cfm?objec...A372F025BF8729

Thanks