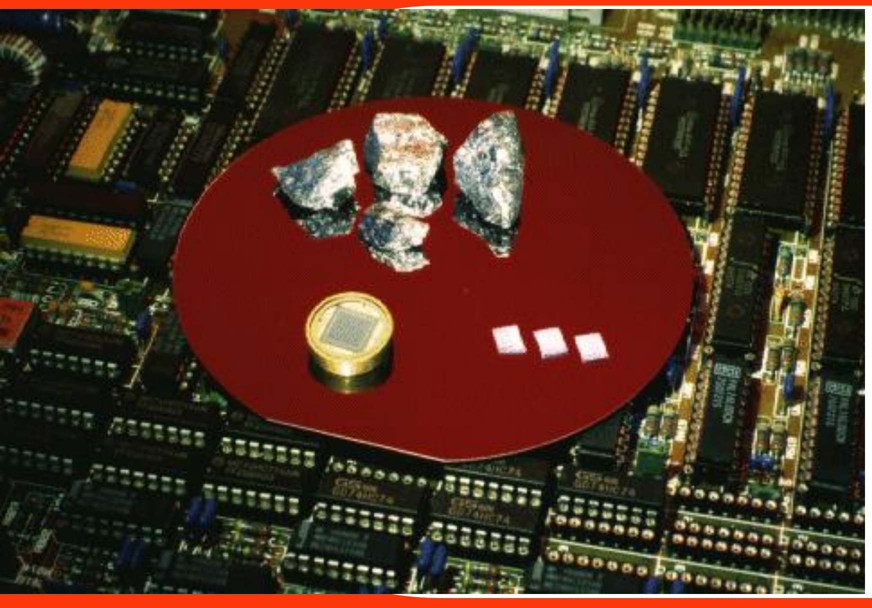


Sustratos
Curso 15-16

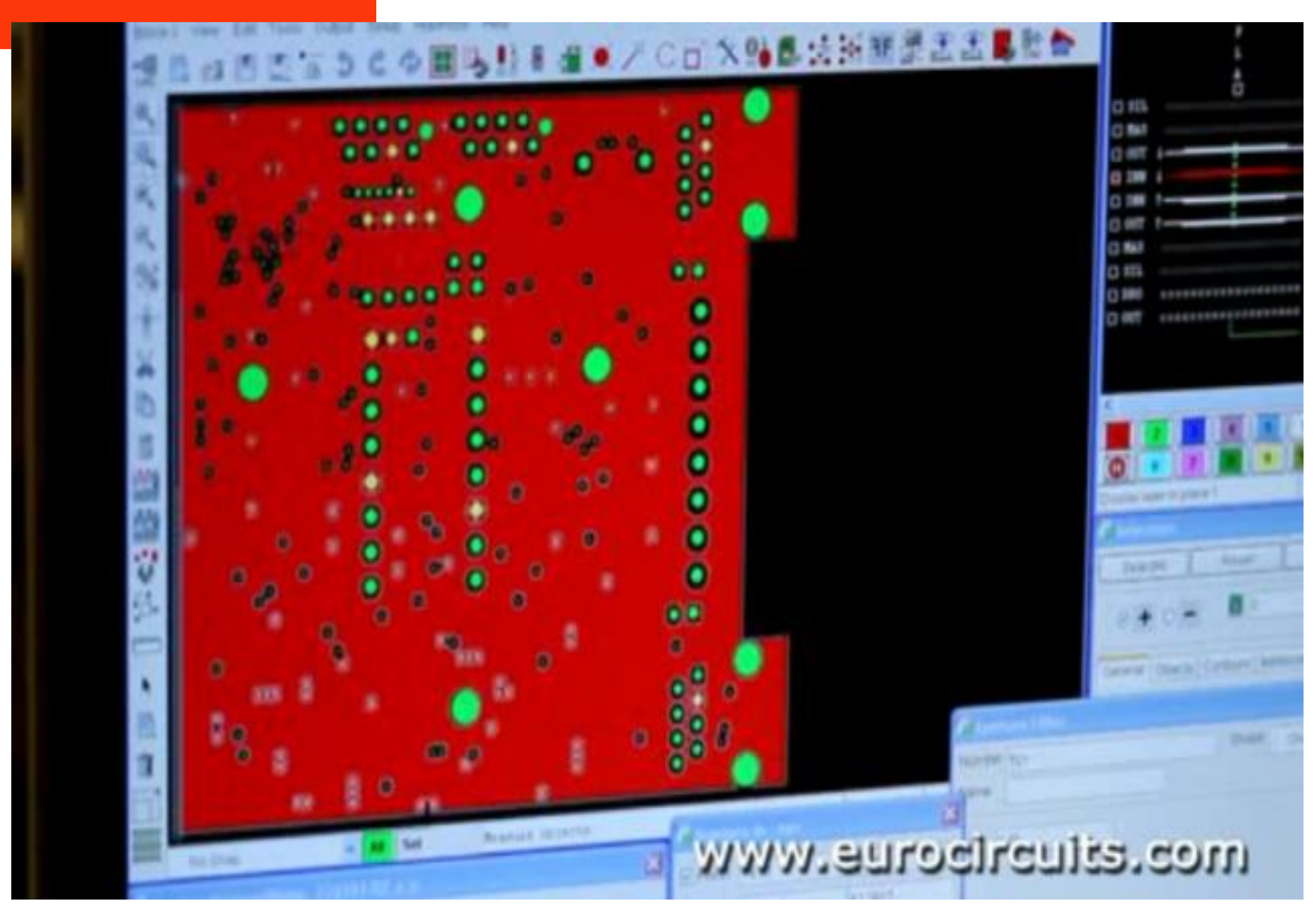
Prof. Andrés Roldán Aranda

4º Curso Grado en Ingeniería de Tecnologías de Telecomunicación

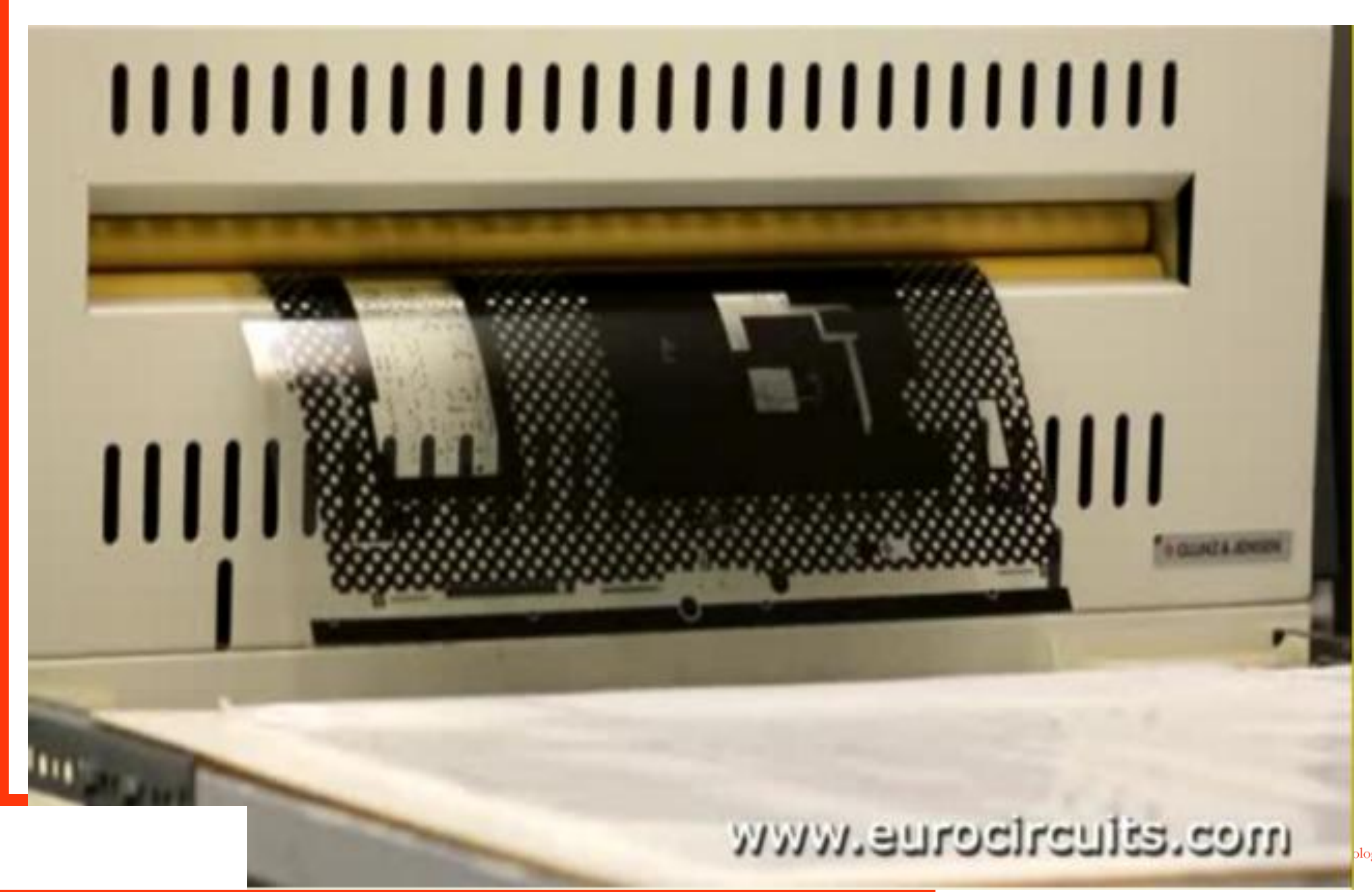
Contenidos

1.- Introducción
2.- Proceso de Fabricación de Placas
3.- Sustratos y tecnologías
4.- Surface Mount Technology
5.- Stencils
6.- Dimensionado de pistas

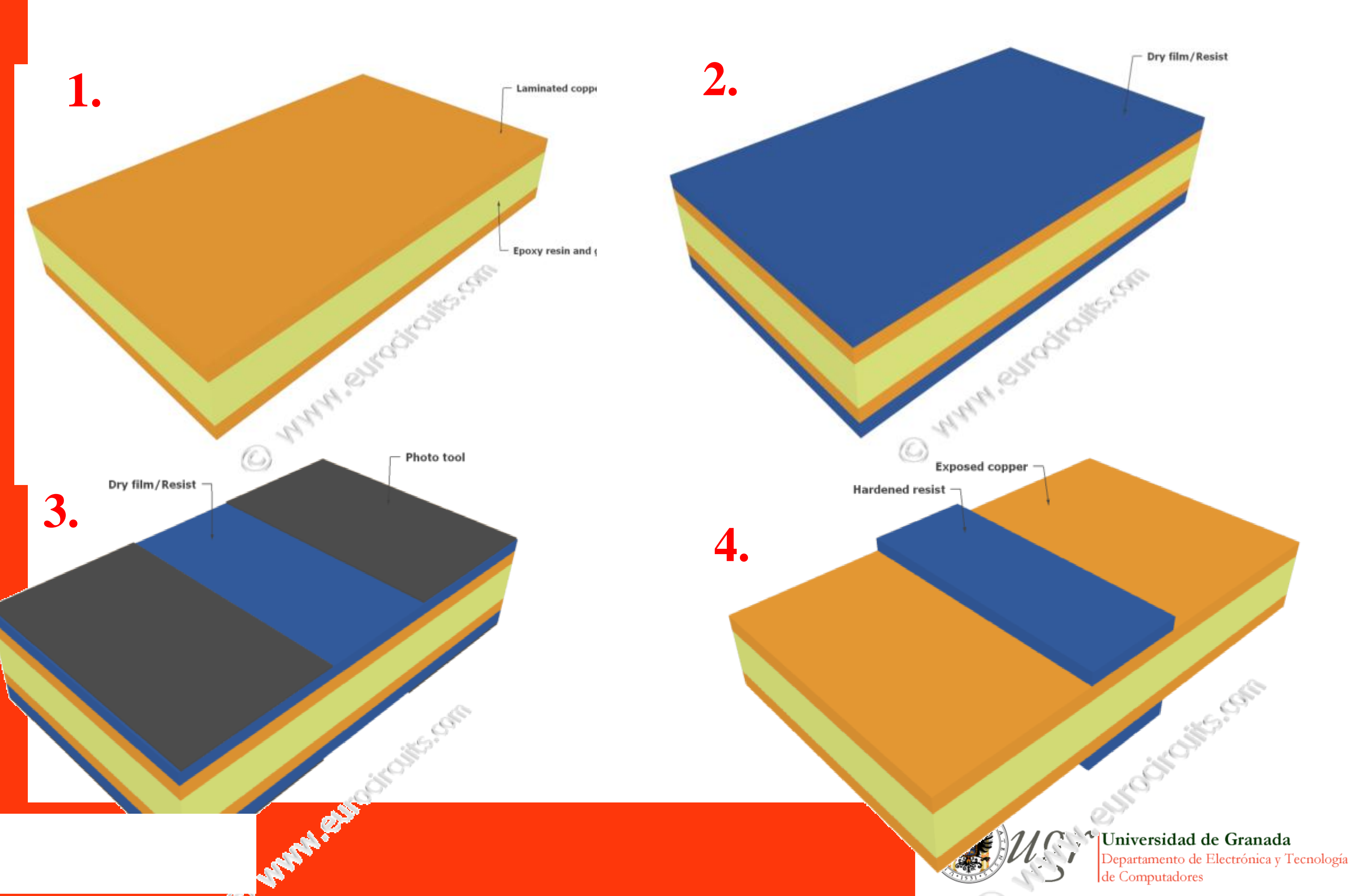
Fase 1: Front-end tool data preparation



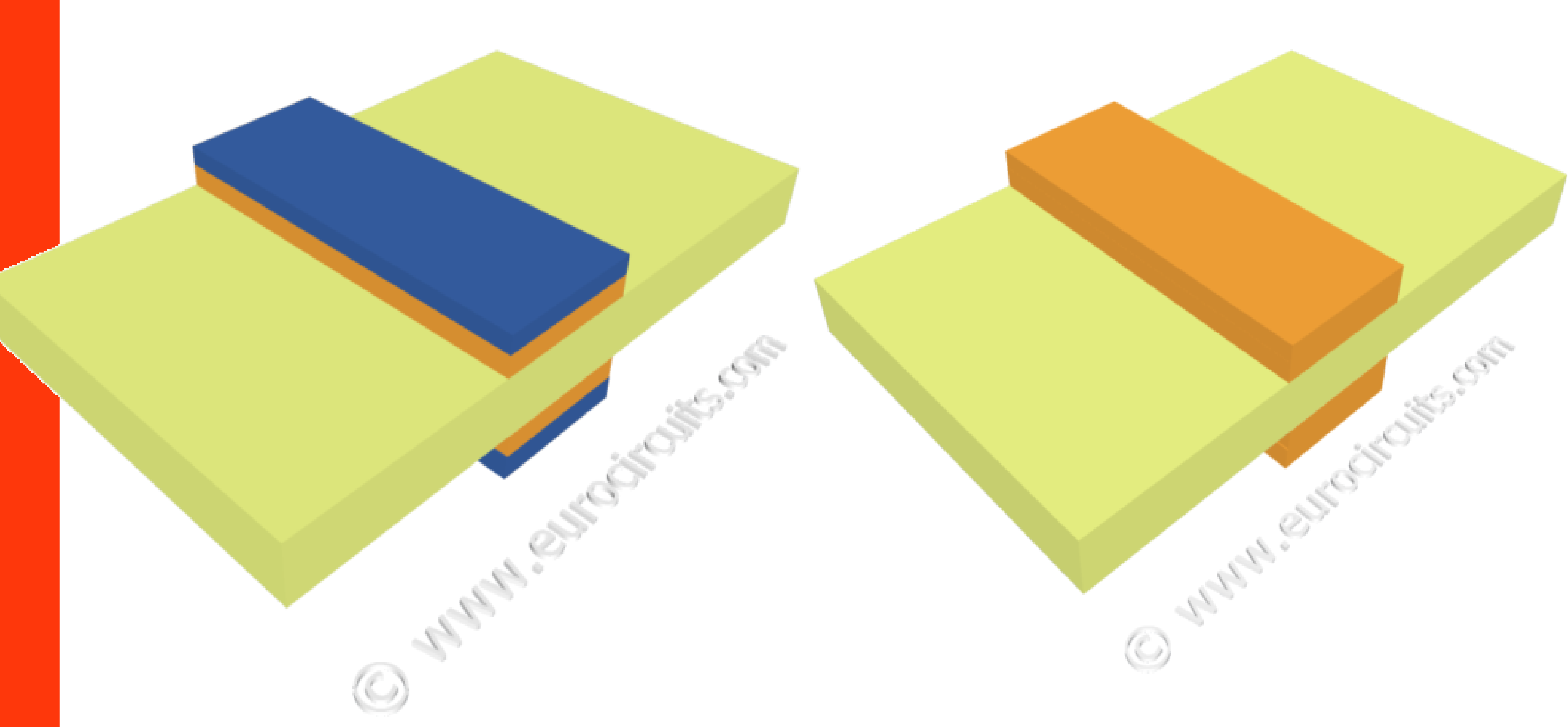
Fase 2: Preparing the phototools



Fase 3: Print inner layers

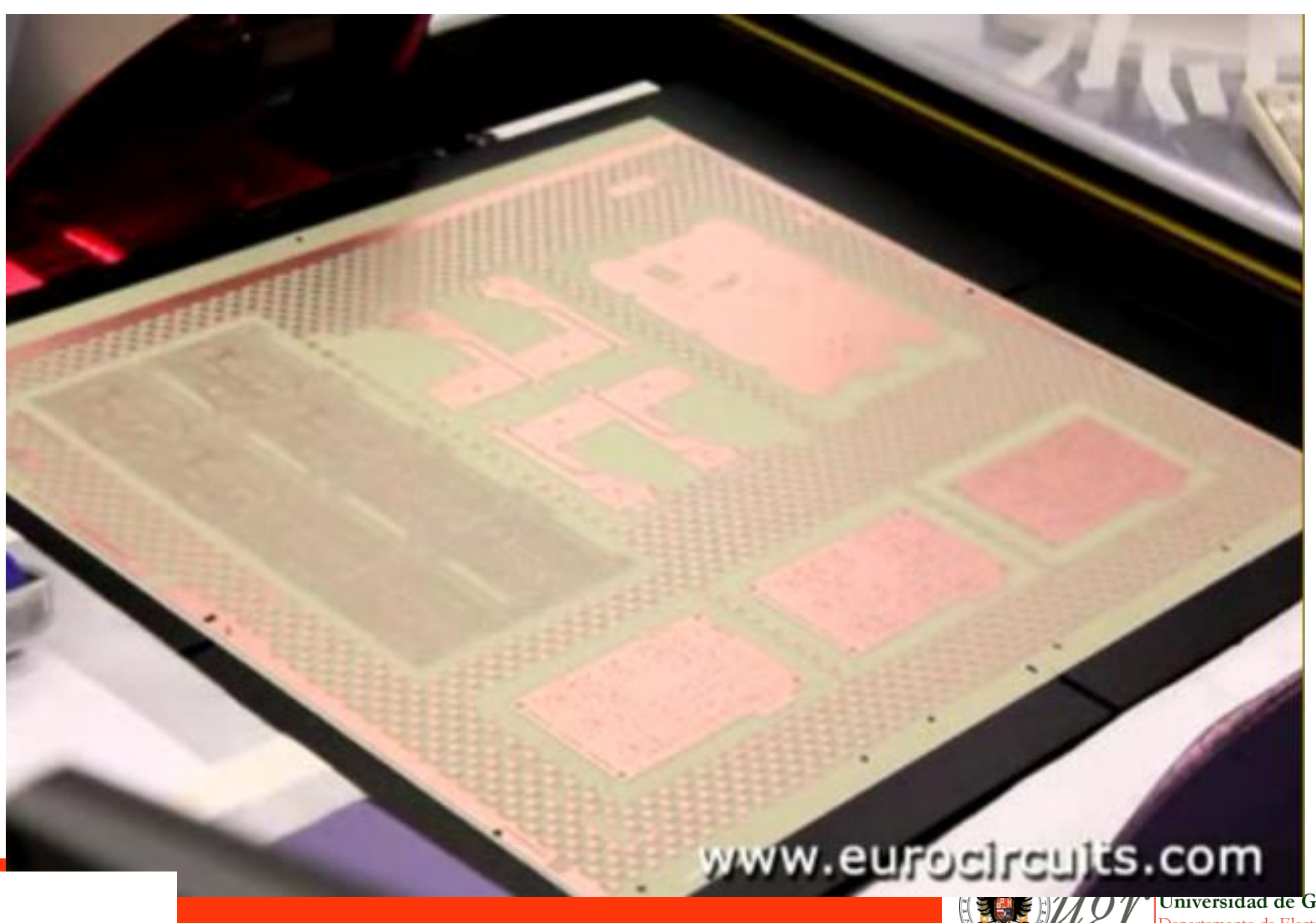


Fase 4: Etch inner layers

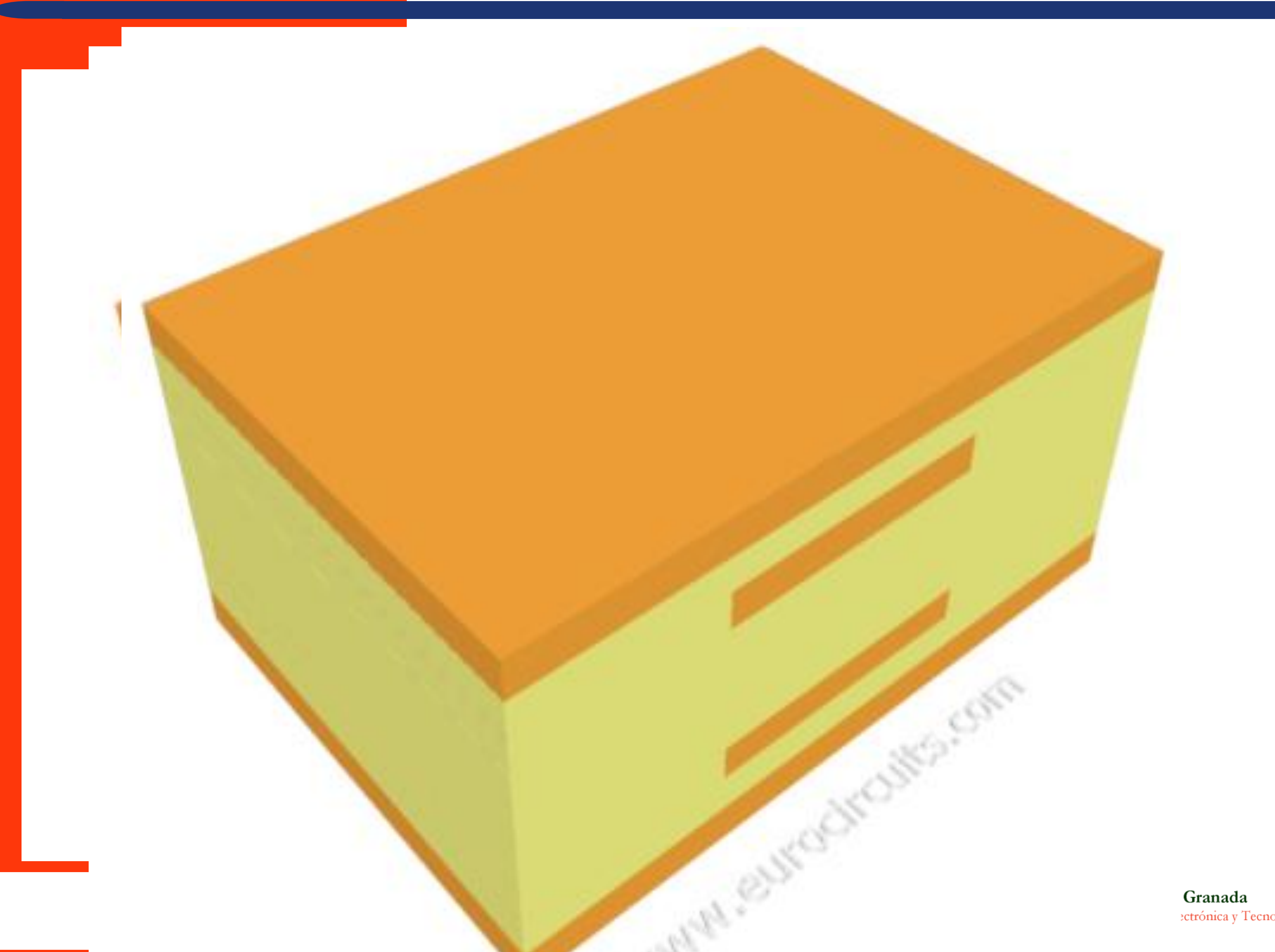


Fase 5:

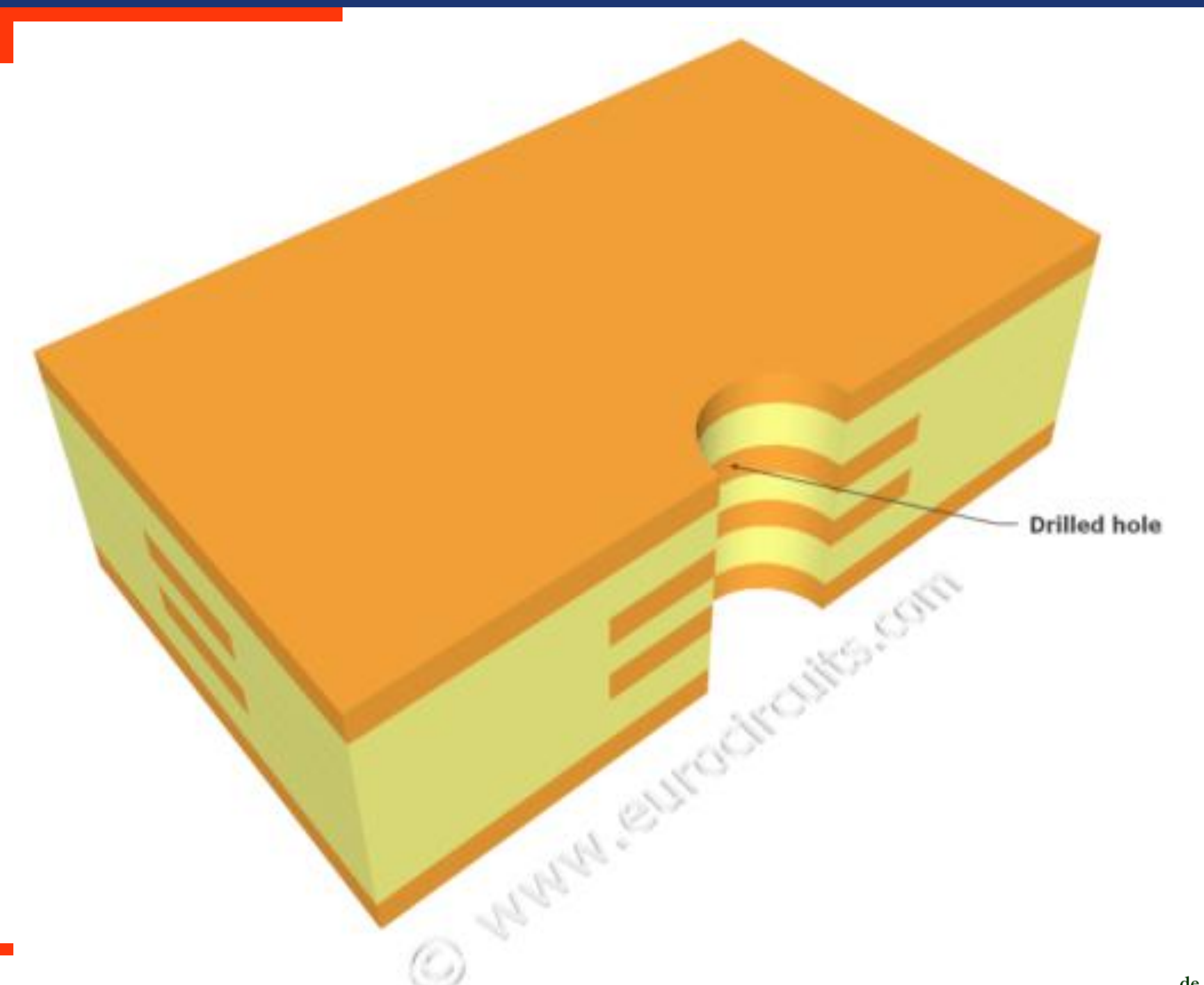
Register punch and Automatic Optical Inspection (AOI)



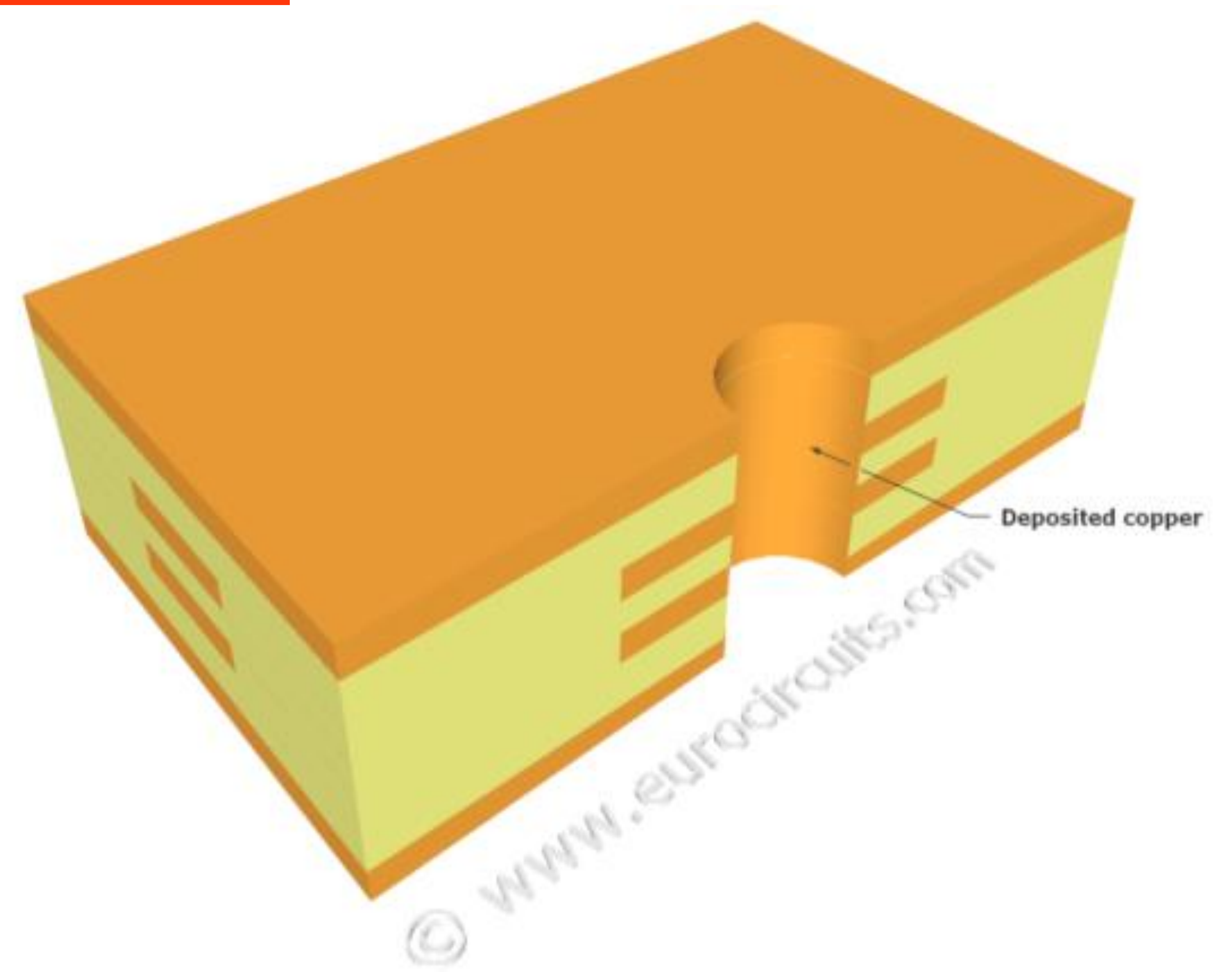
Fase 6: Lay-up and bond



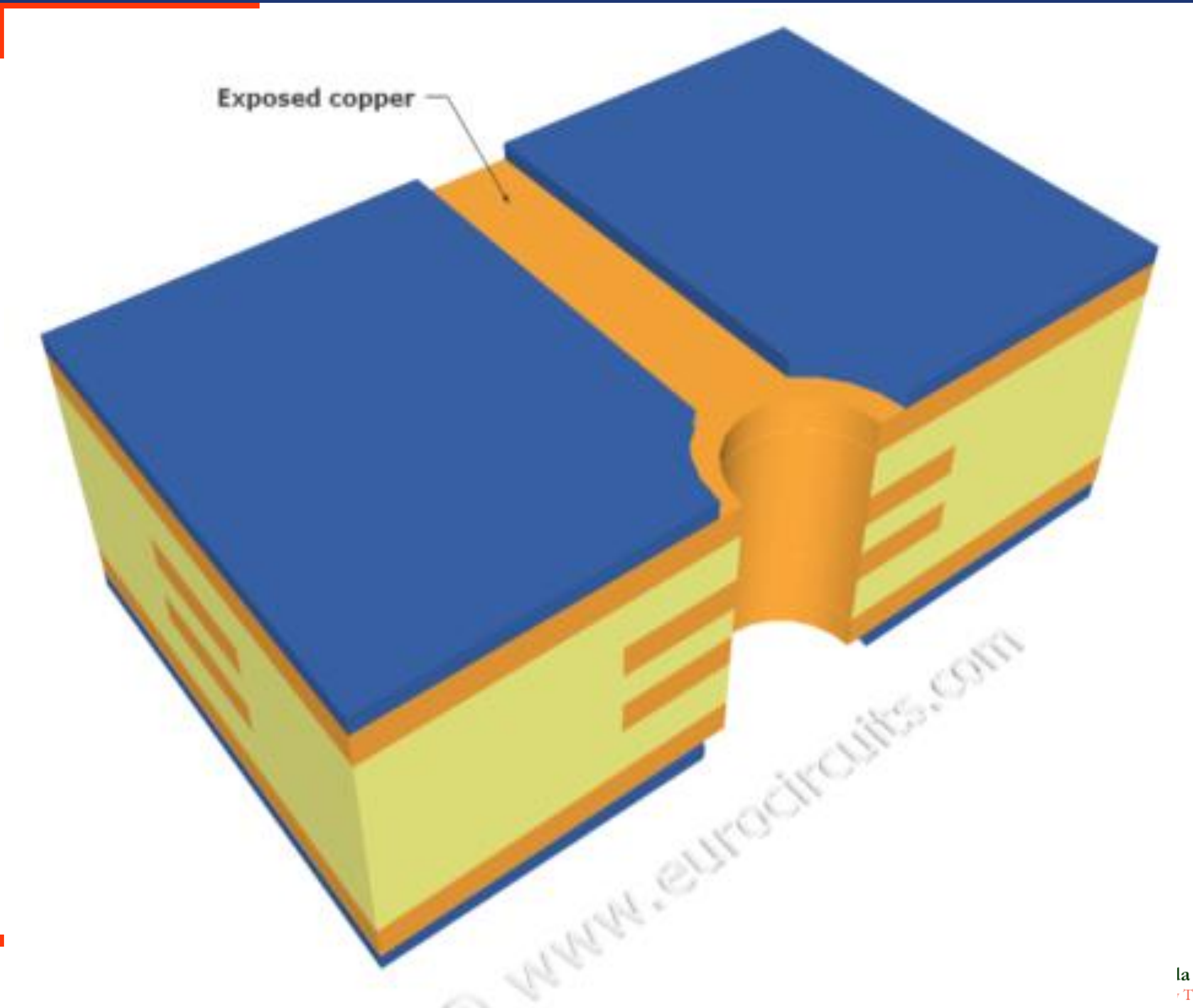
Fase 7: Drilling the PCB



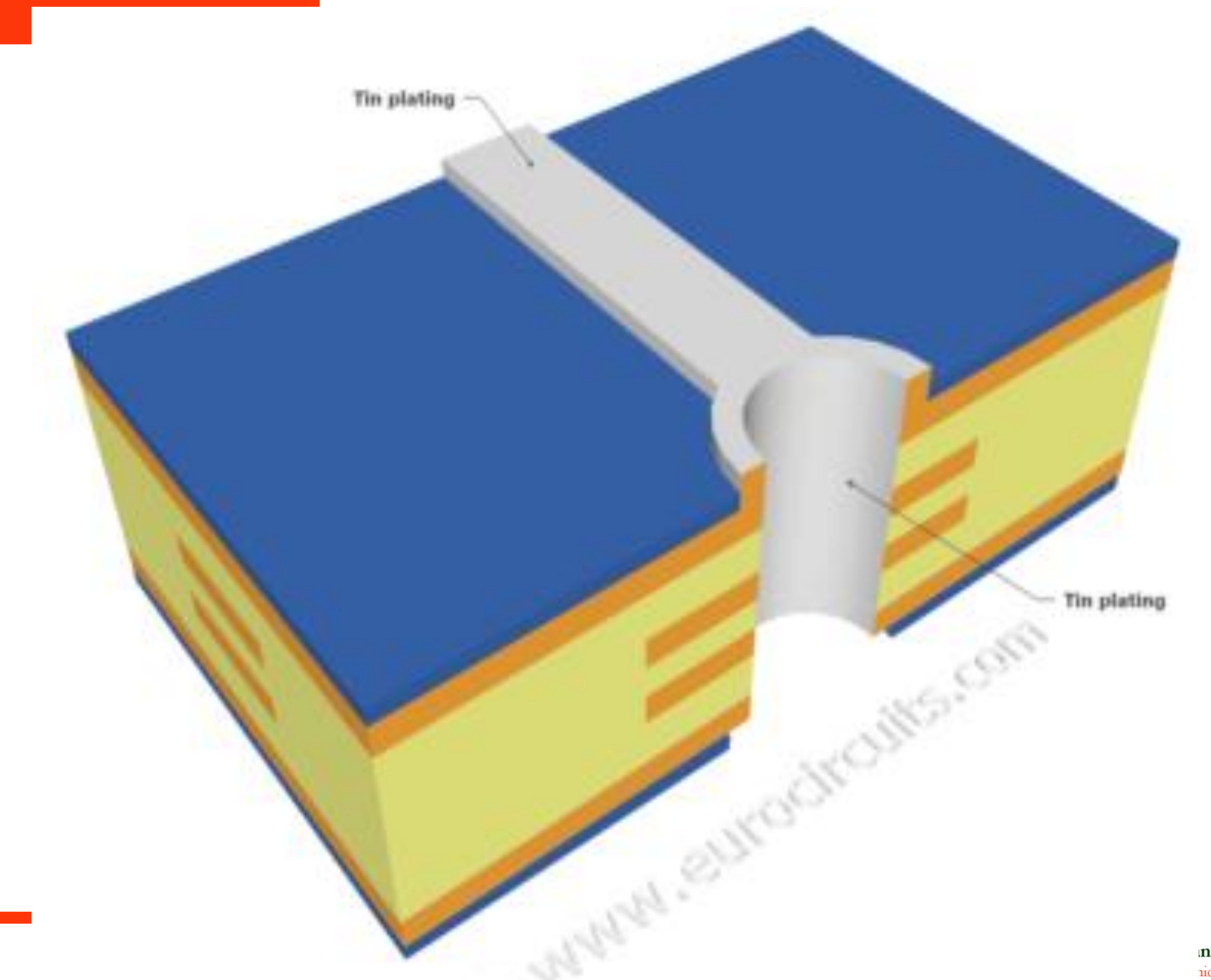
Fase 8: Electroless copper deposition



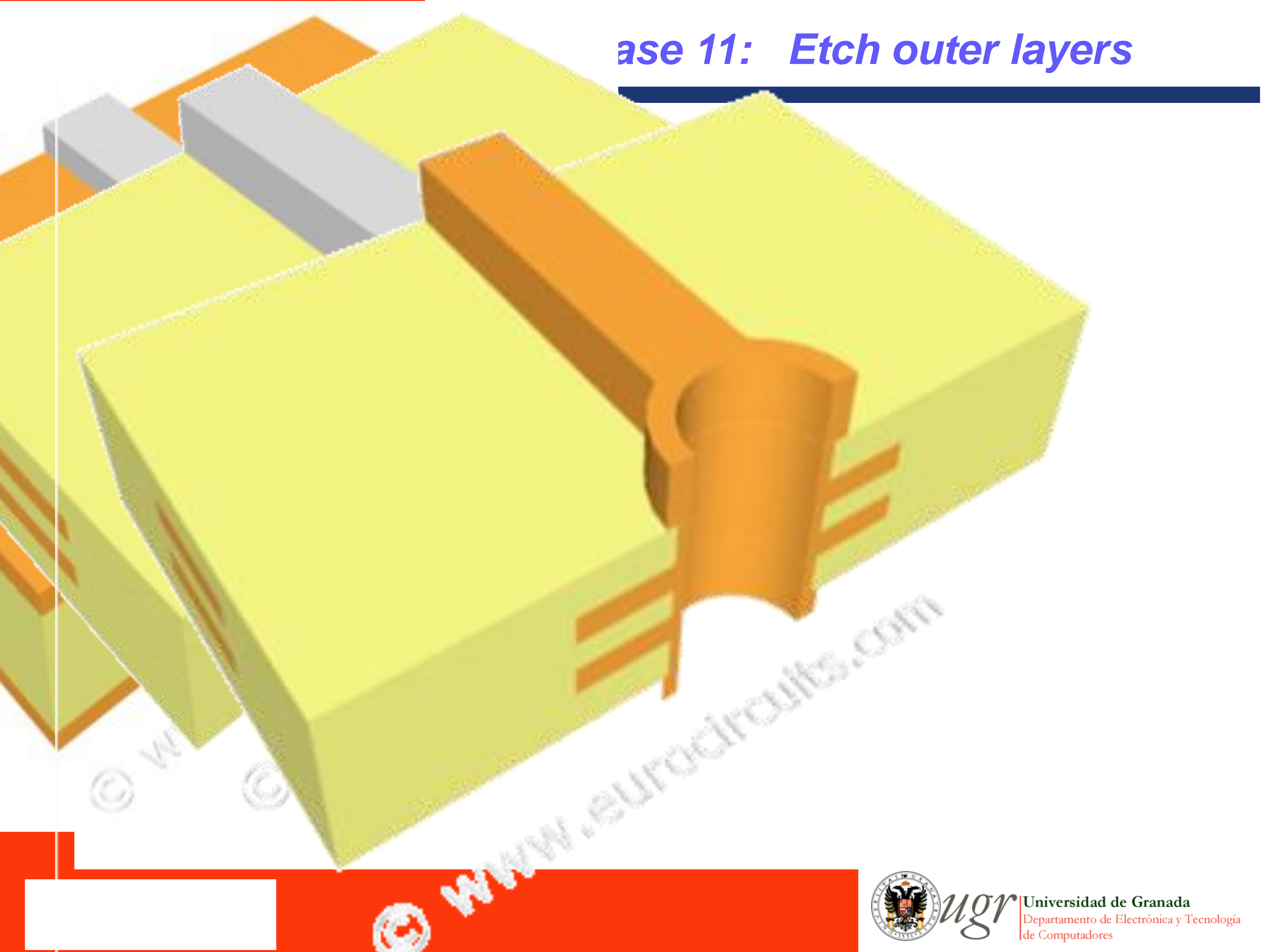
Fase 9: Image the outer layers



Fase 10: Electroplate the boards with copper



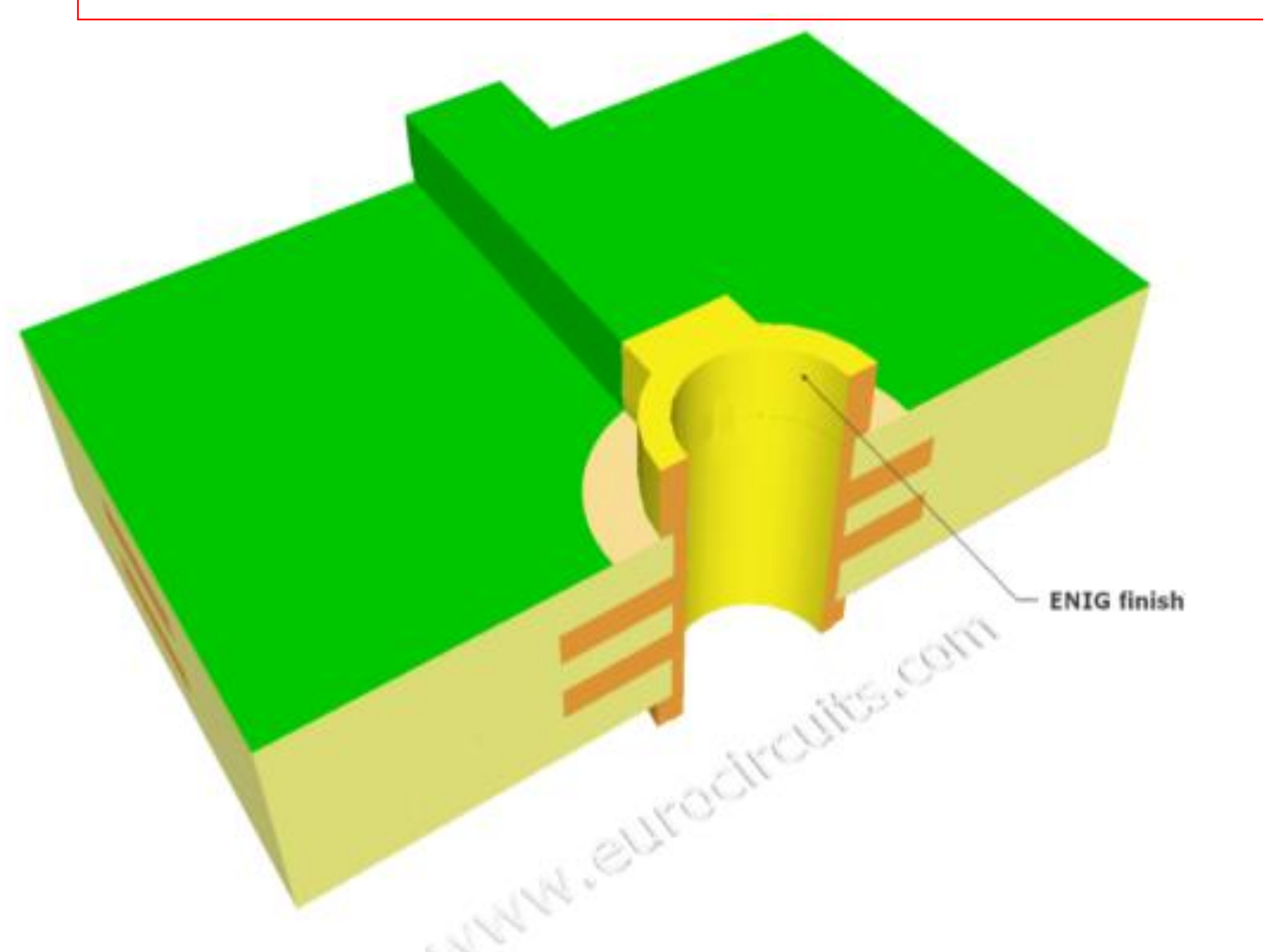
ase 11: Etch outer layers



Fase 12: Apply soldermask

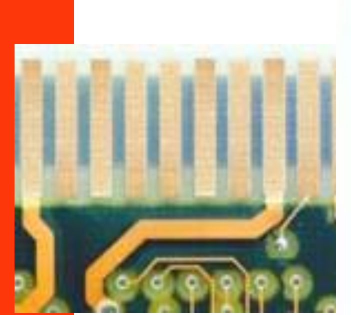
Fase 13: RoHS-compliant surface finishes – electroless gold over nickel

RoHS : Reduction of Hazardous Substances



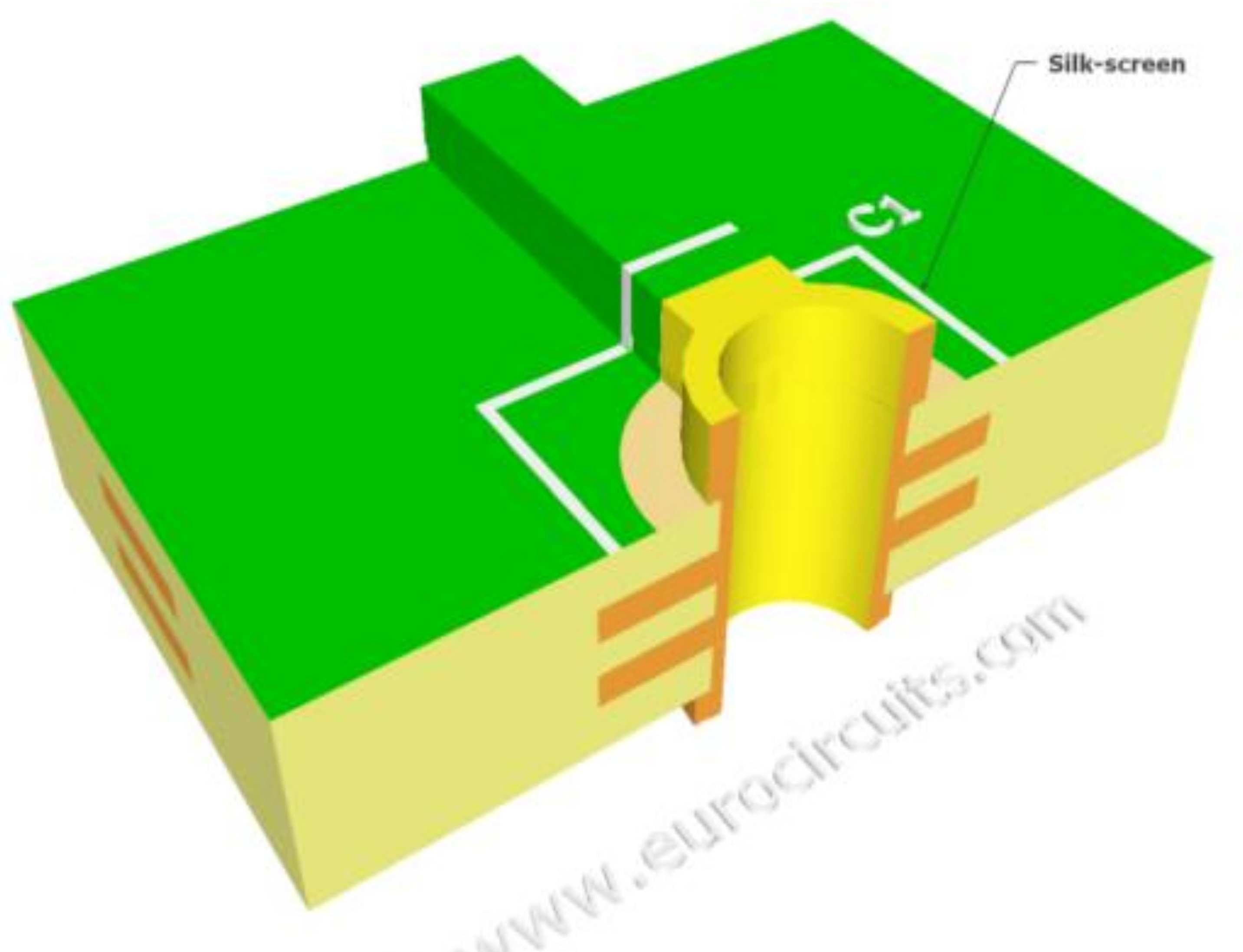
Fase 14: Plated Hard-gold edge connectors

electro-plate 1 – 1.5 microns of gold over 4 – 5 microns of plated nickel



Fase 15: Silk-screen and cure

Ink-jet image printing needs no set-up.
10 minutes using a 5 stage conveyorised oven



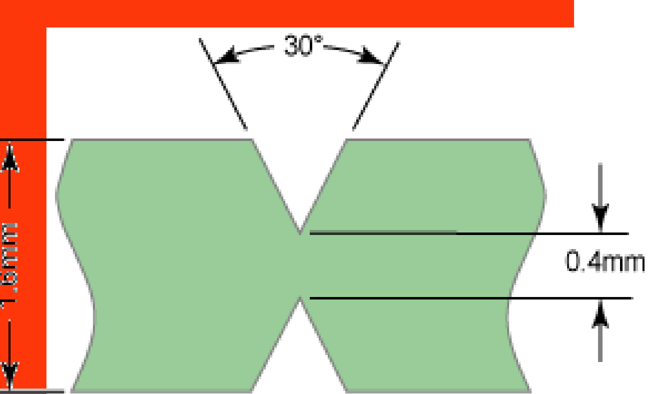
Fase 16: Electrical test

Test speed 25,4 mm/s
With 4096 test pins

The scan consists of thousands of **0.1mm** diameter probes, gentle as a human hair, brushing over the PCB, producing an electrical picture as they scan.

Using a flying probe tester we check each net to ensure that it is complete (no open circuits) and does not short to any other net

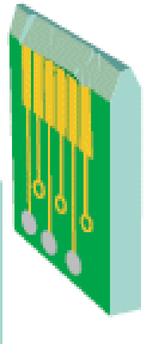
Fase 17: Profiling. V-Cut scoring



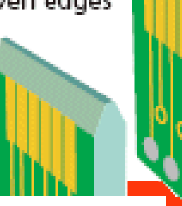
- misregistration from top-side score to bottom-side score to be ±0.1mm
- residual matter thickness after scoring to be 0.4mm ±0.1mm
- top-side and bottom-side score depths should be even, to within 0.2mm of each other
- v-score to run the entire length of the panel
- the v-score should not cut any copper

Filing often causes scuffing and undercut of substrate

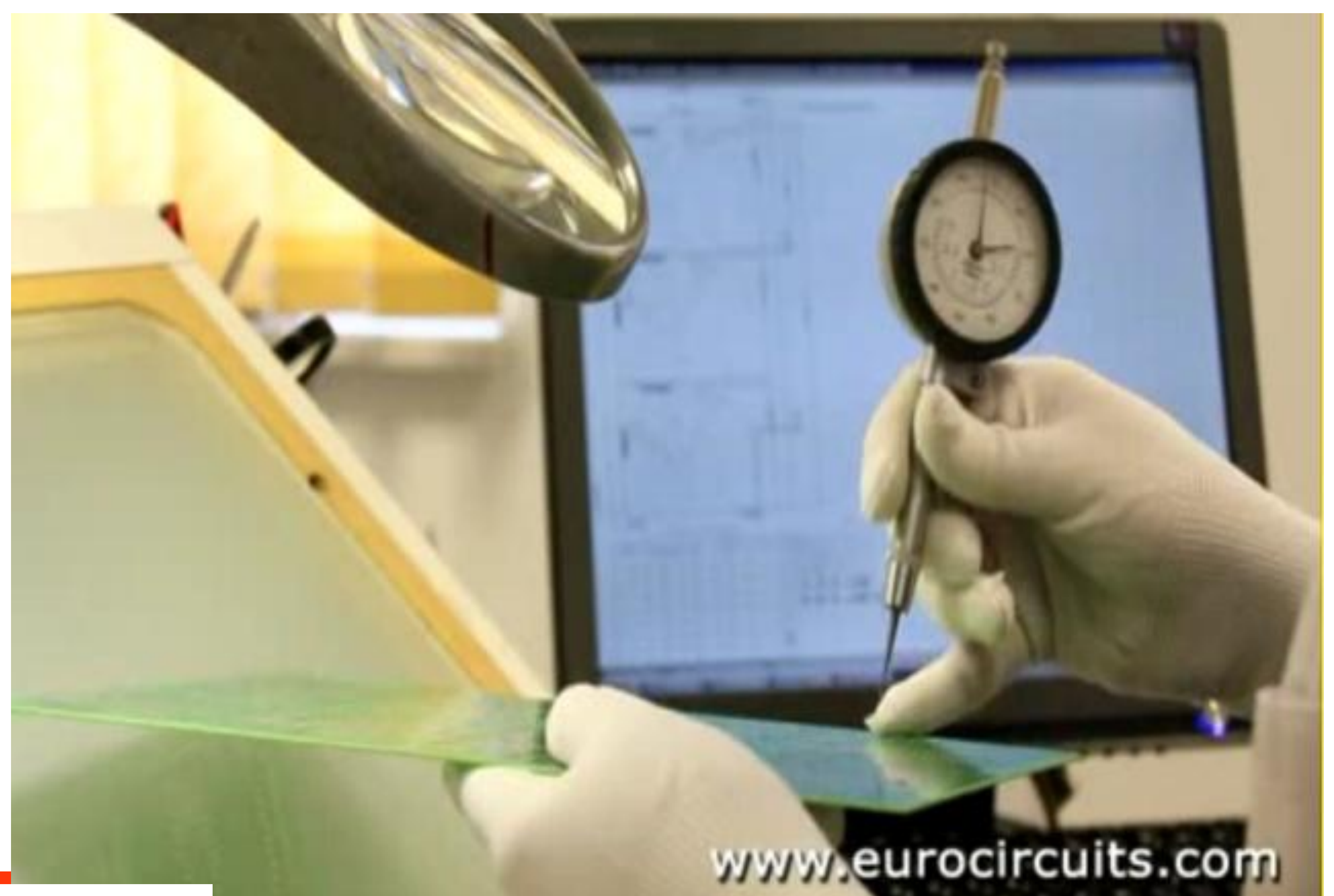
Linishing can lift delicate circuitry & produce uneven edges



EdgeCut produces a controlled profile



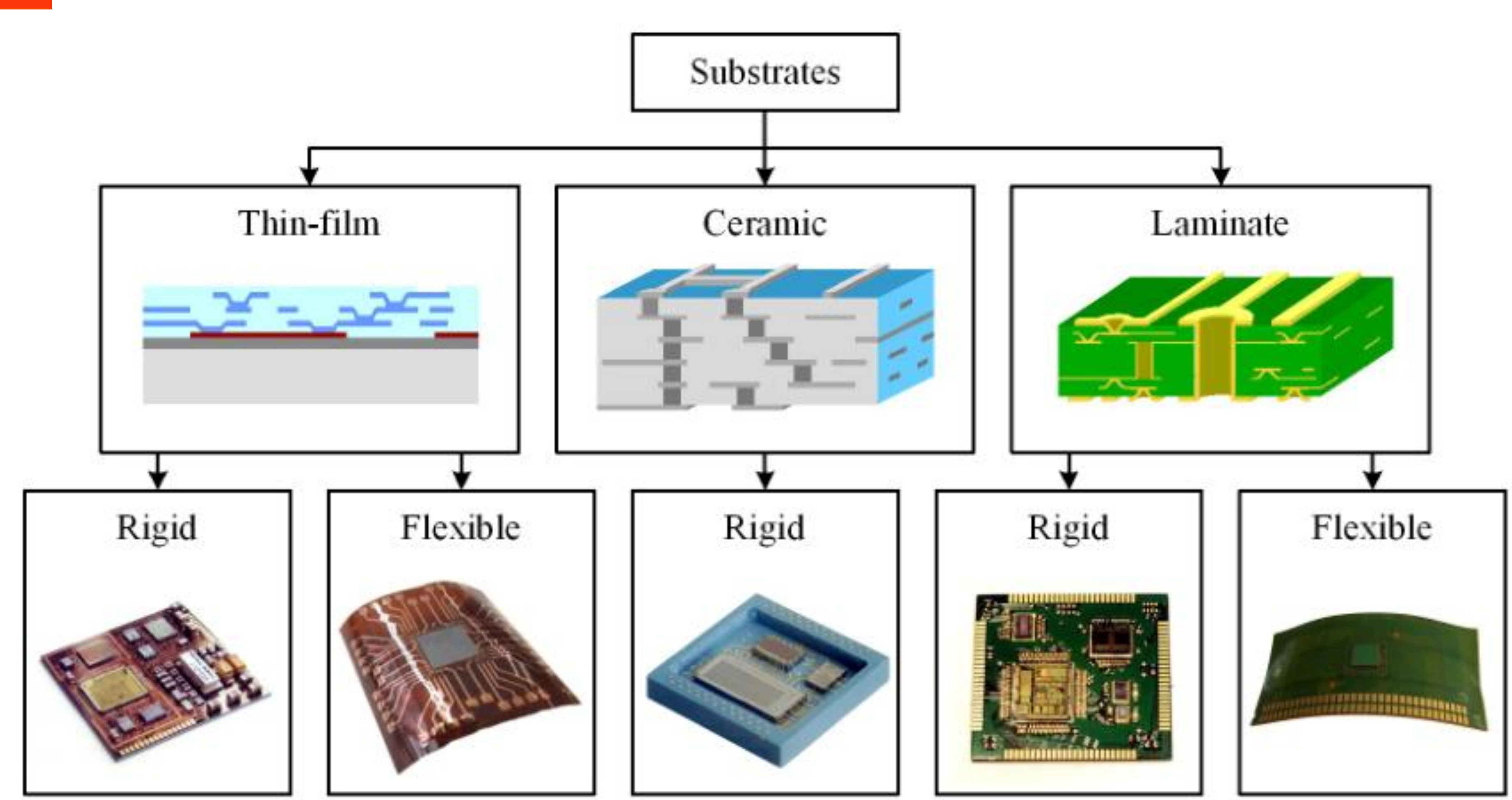
Fase 18: Final inspection - vacuum-sealed to keep out dirt and moisture



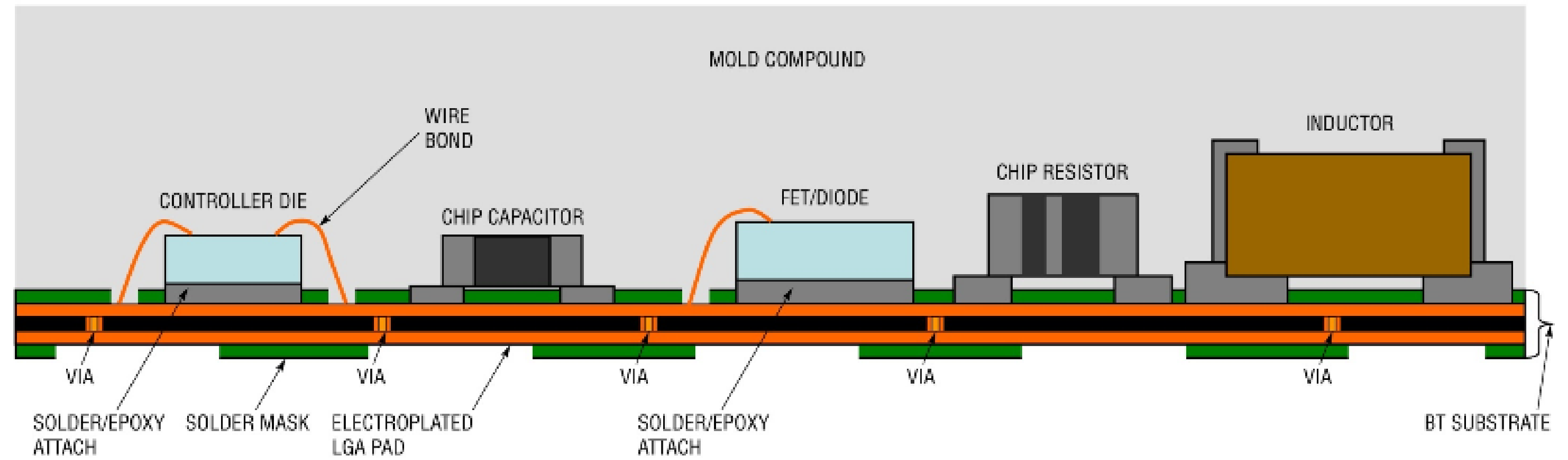
Watch a VIDEO

Video

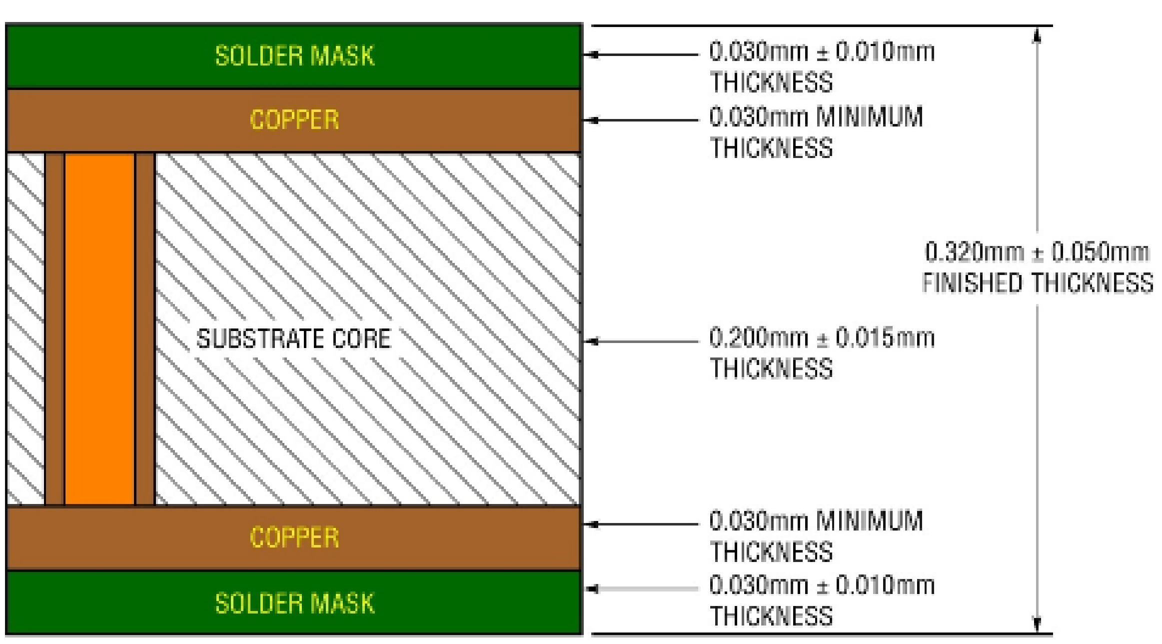
Substrate Technologies



LGA Module Construction



Substrate Construction



All dimensions in mm

LTM4600 HIGH PERFORMANCE SUBSTRATE

Ni/Au Plating

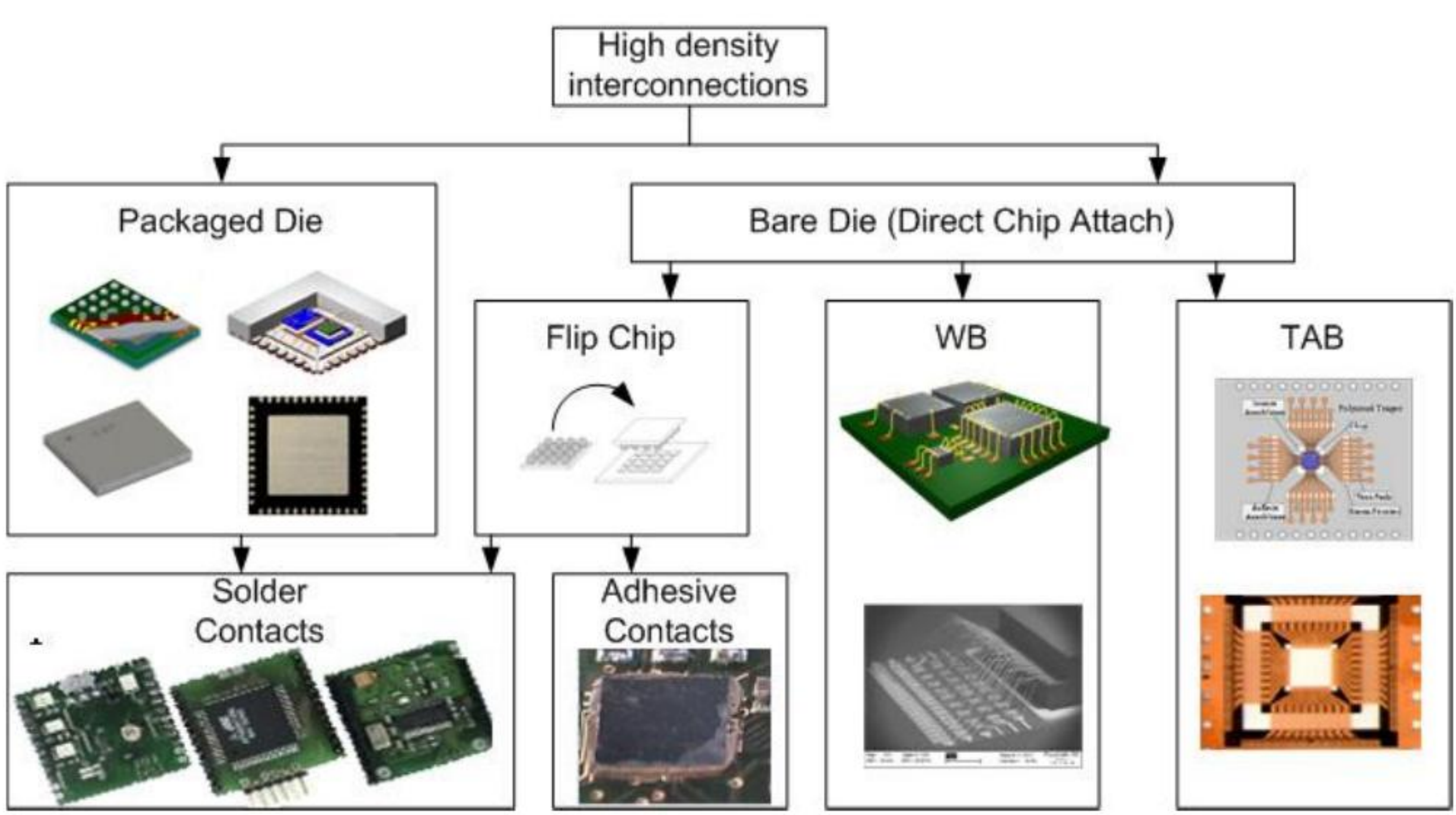
SOLDER MASK = Taiyo ink PSR 4000

CORE = Mitsubishi Gas Chemical CCL-HL-832

Ni= 3 um minimum (5 um nominal)

Au = 0.3 to 0.8 um (0.5um nominal)

2D Module Integration Technologies



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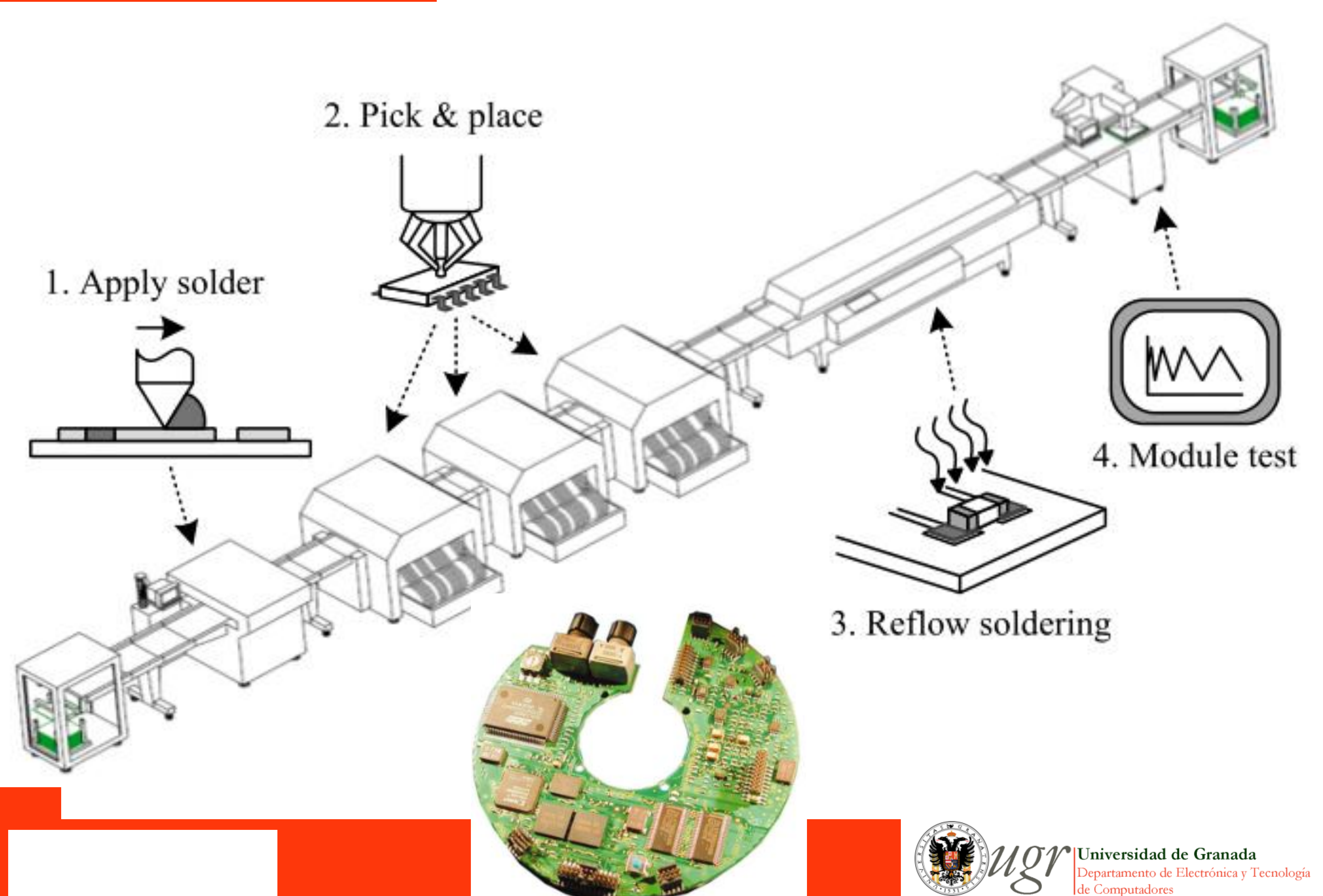
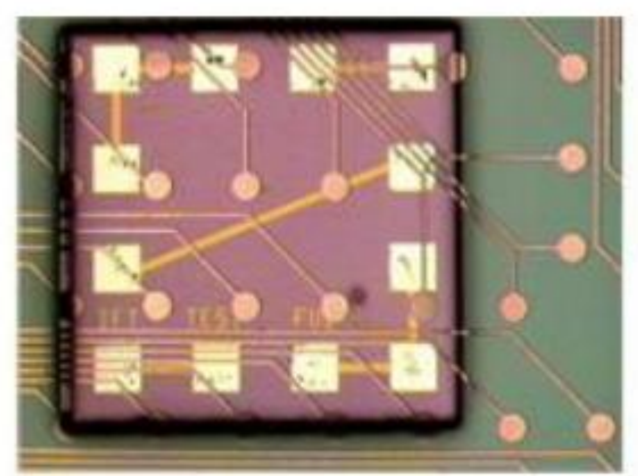
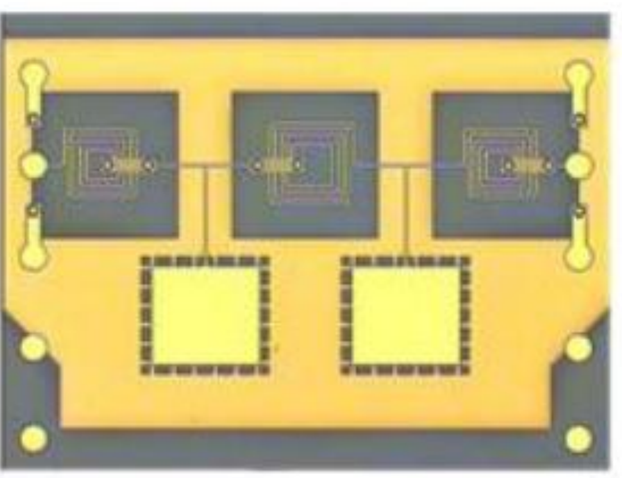
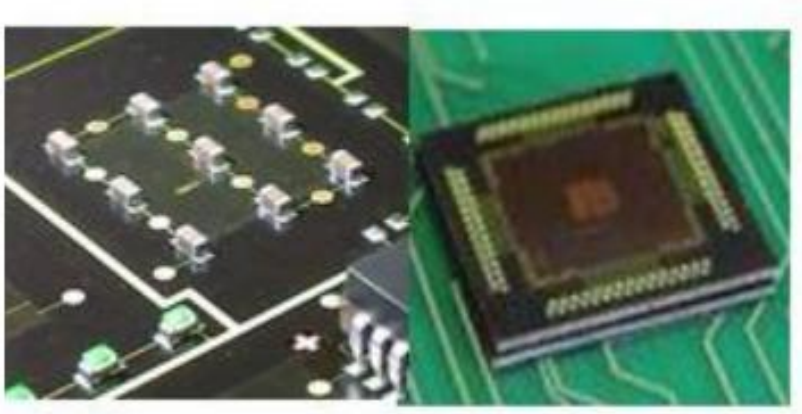
Surface Mount Technology

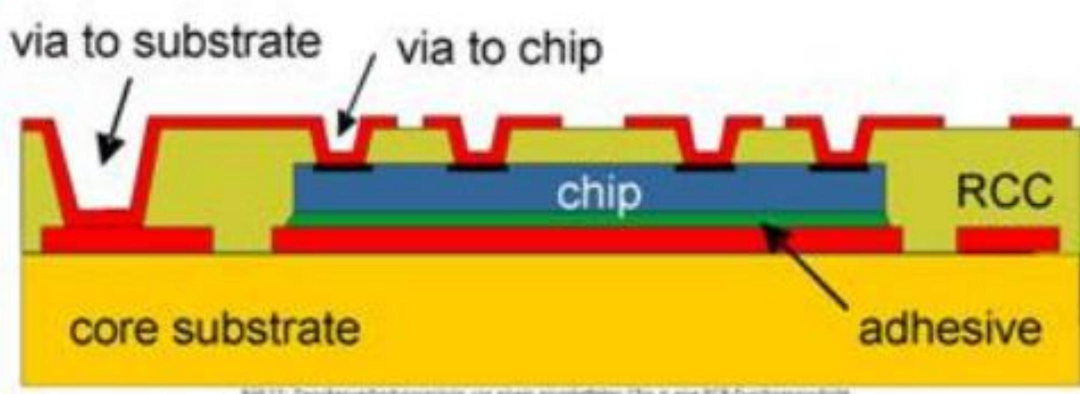


Embedding Components









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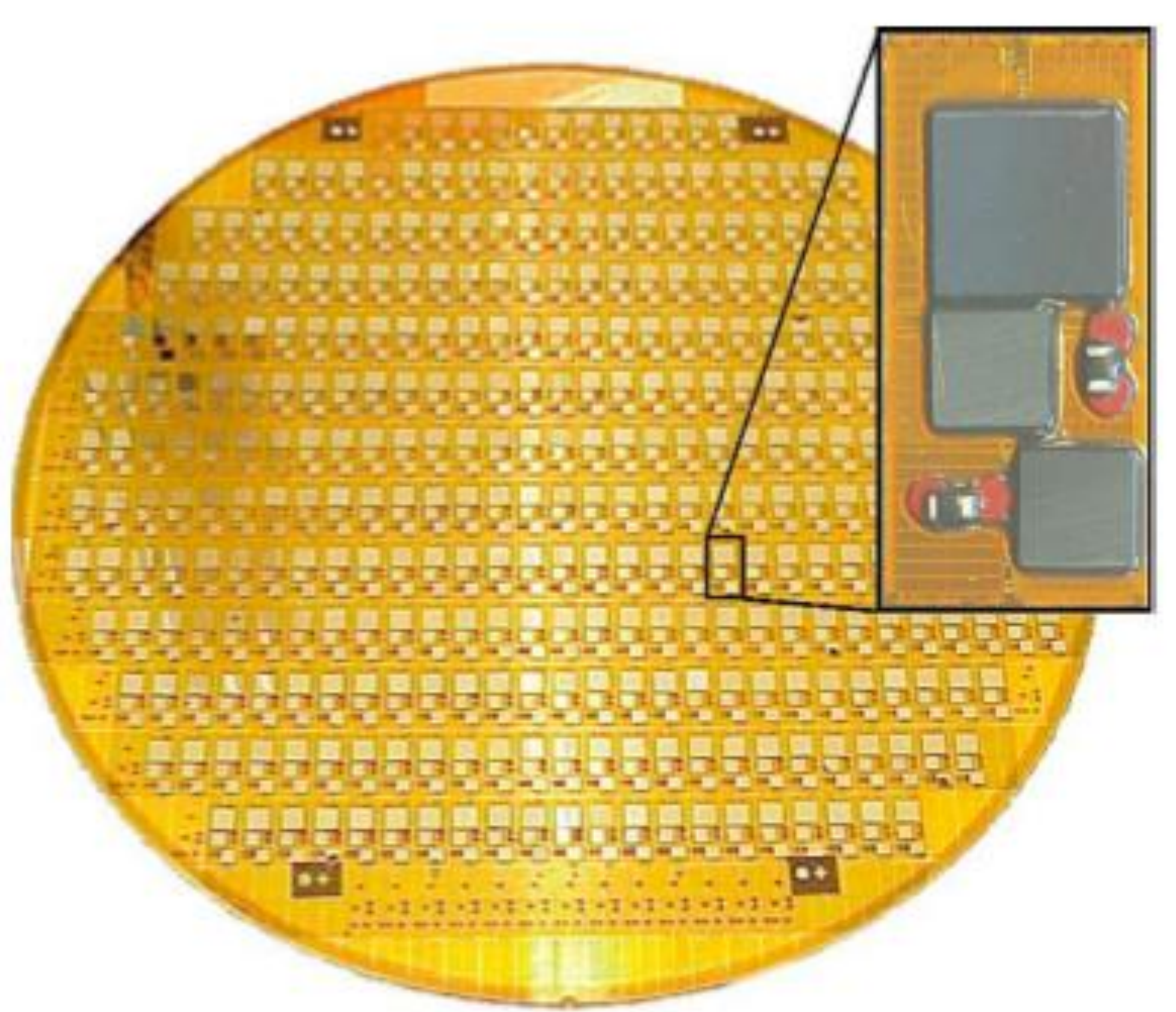
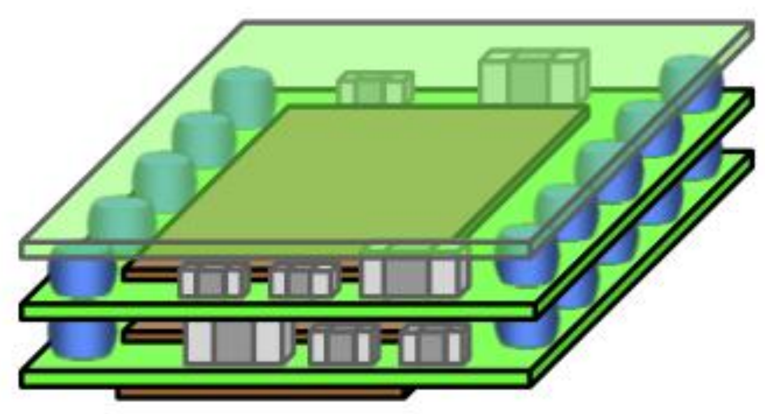
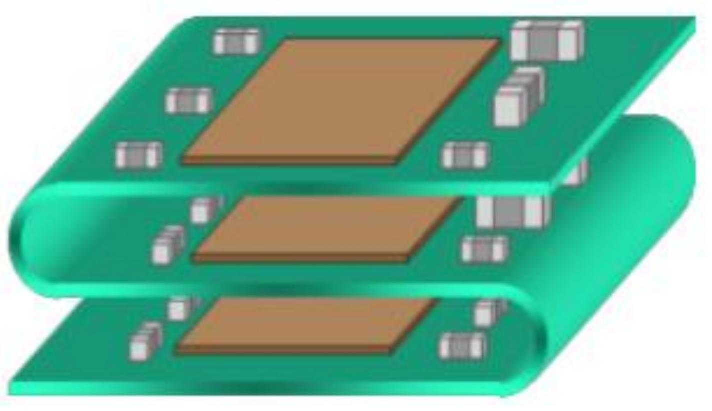
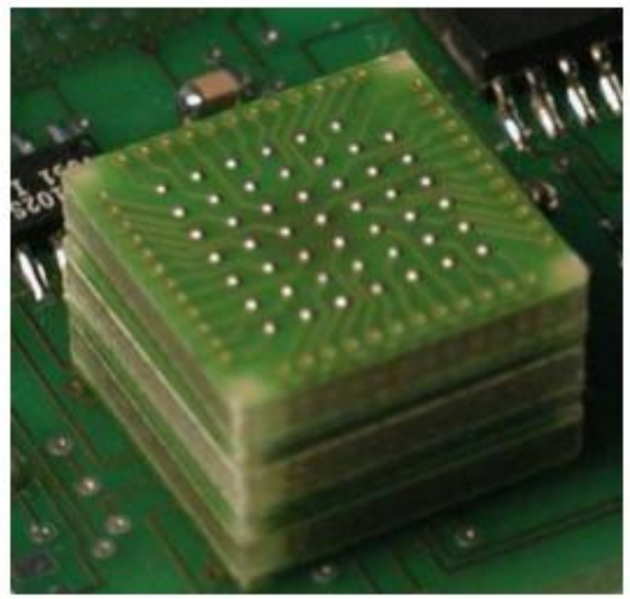
Wafer level integration

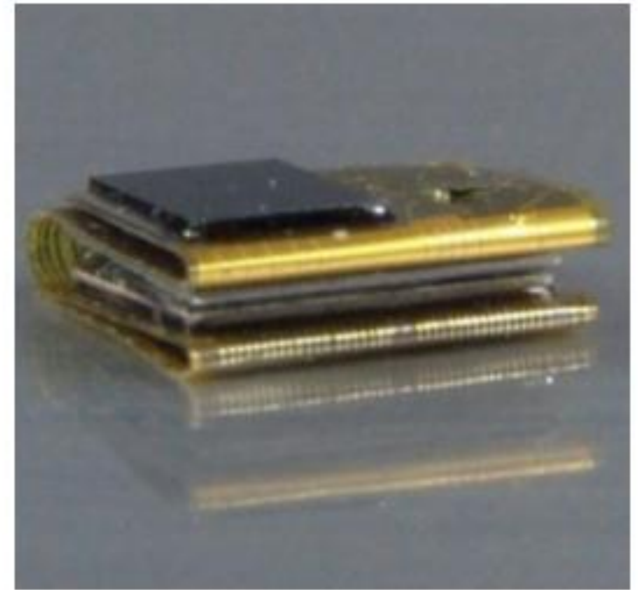


3D Model Integration

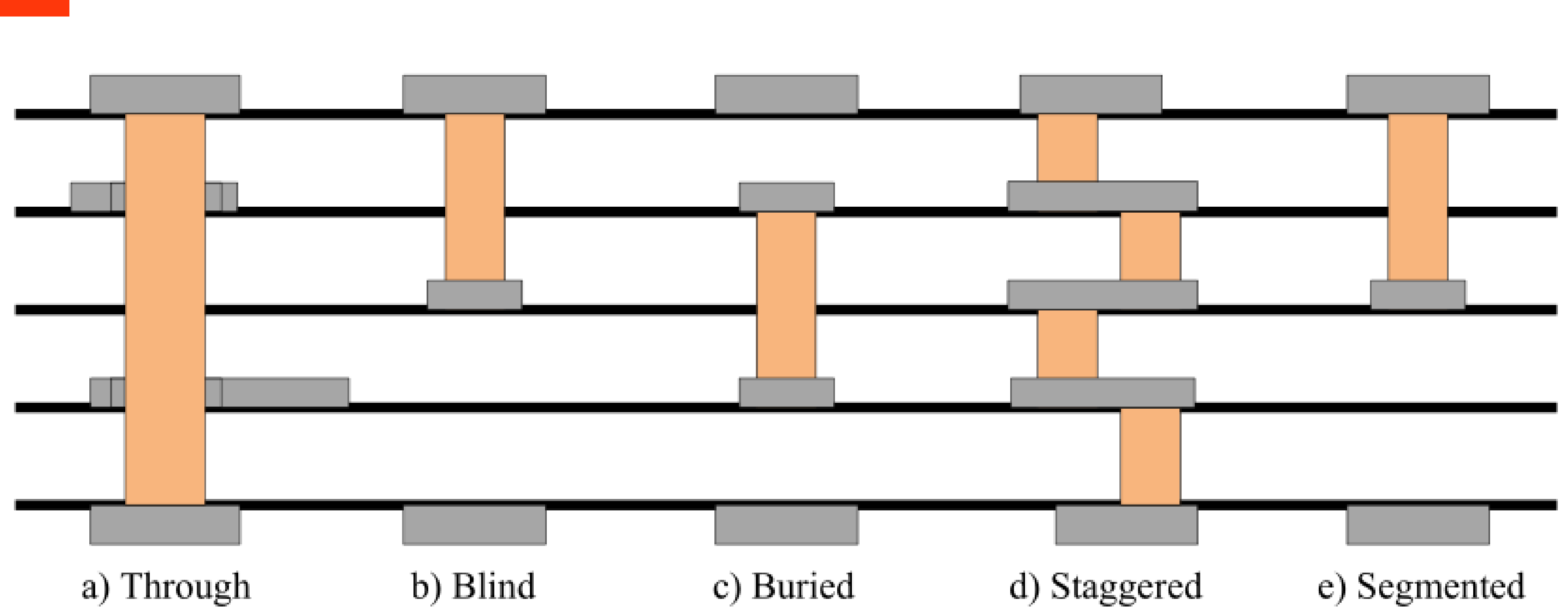




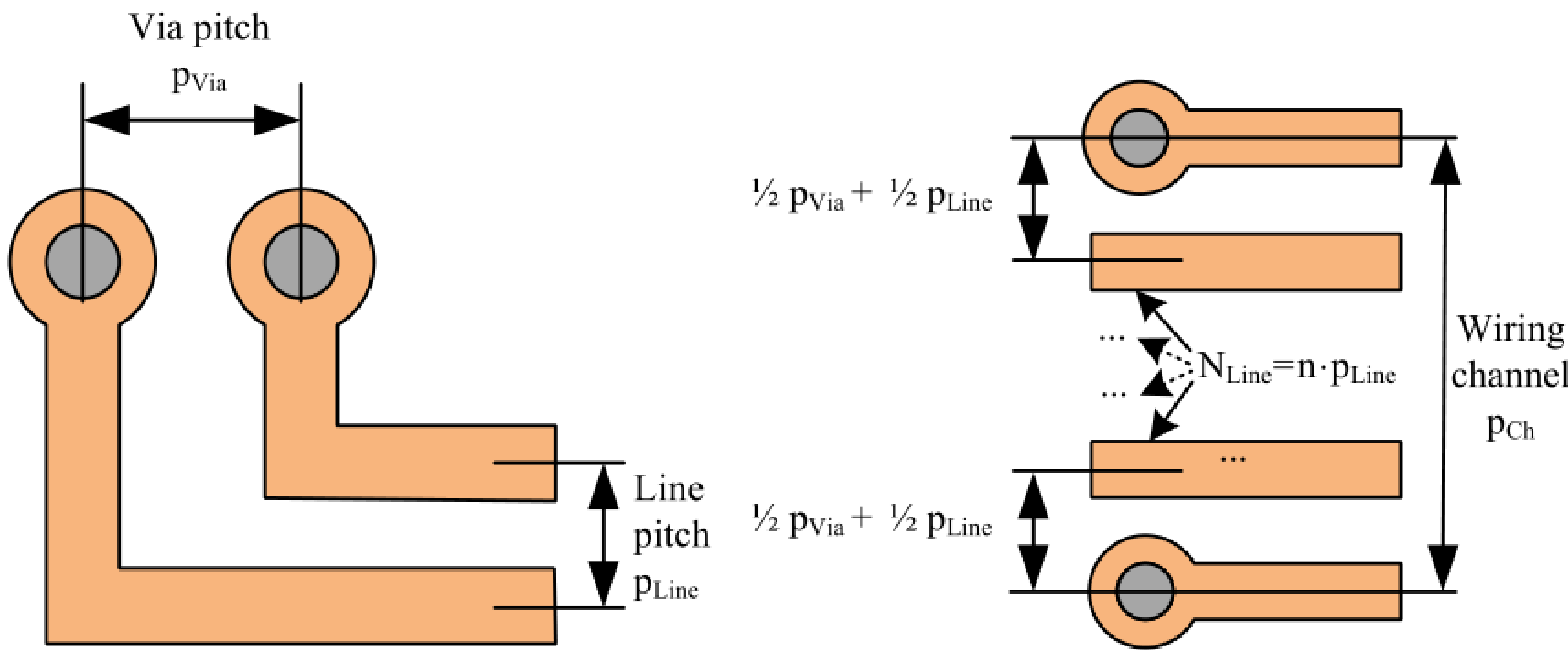




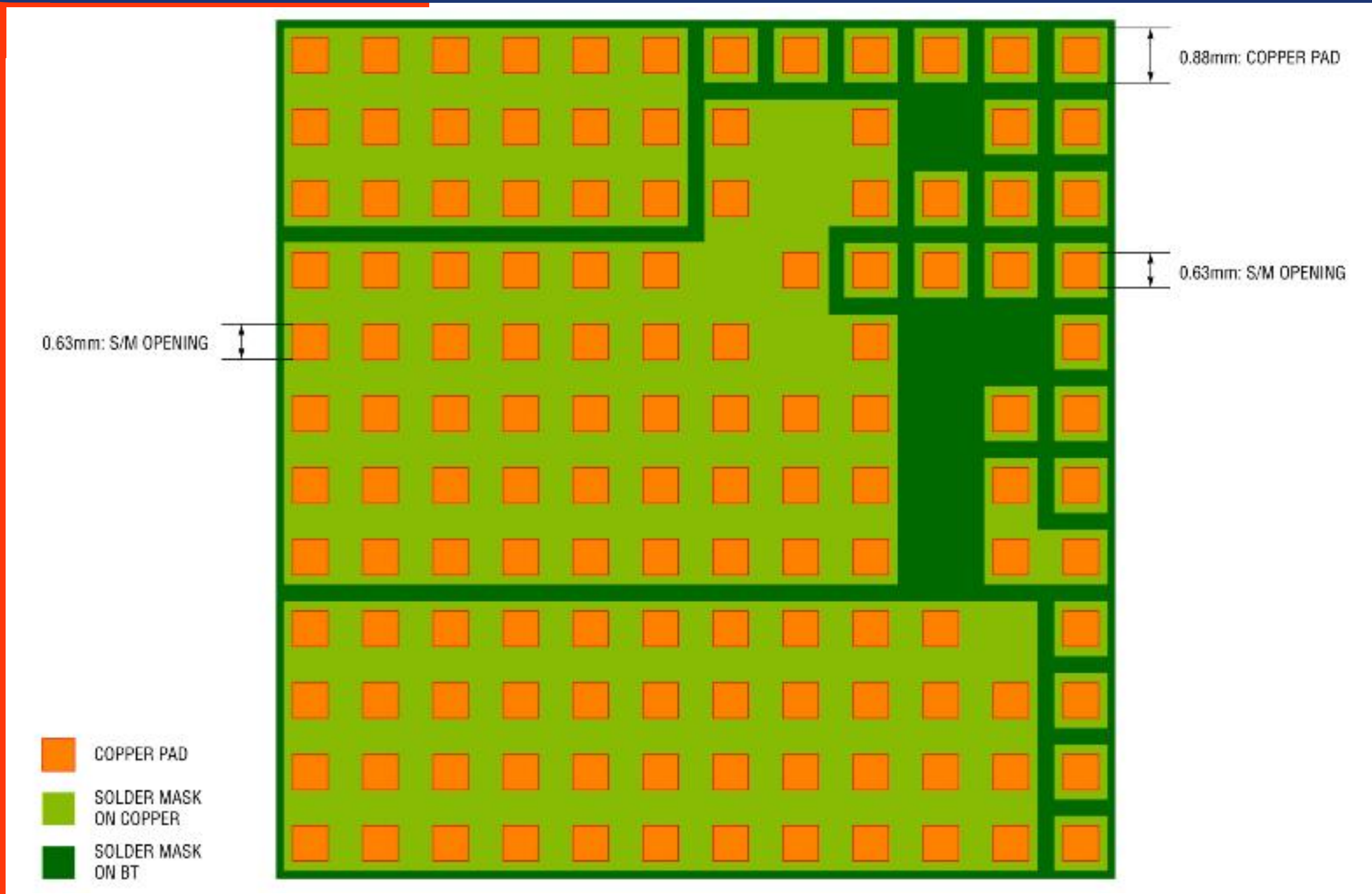
Via Types



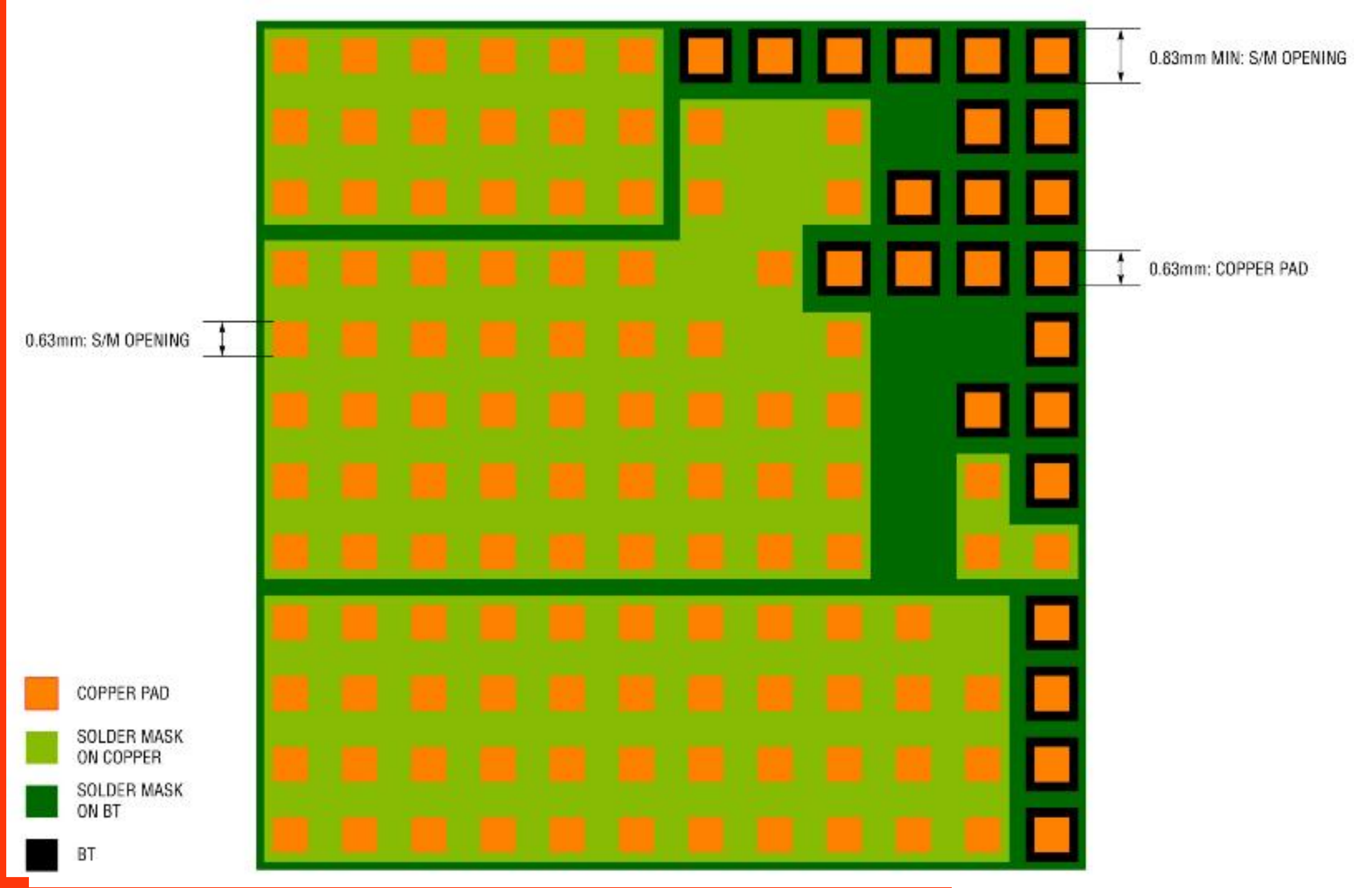
Via Pitch and Wiring Channel



Solder Mask Defined Pads



Linear Technology Corporation Mixed Pads (SMD and NSMD)



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Thermal Relief: NSMD

0.83 MIN: S/M OPENING

0.83 MIN: S/M OPENING

0.63mm: COPPER PAD

0.63mm: COPPER PAD

COPPER PAD

SOLDER MASK ON COPPER

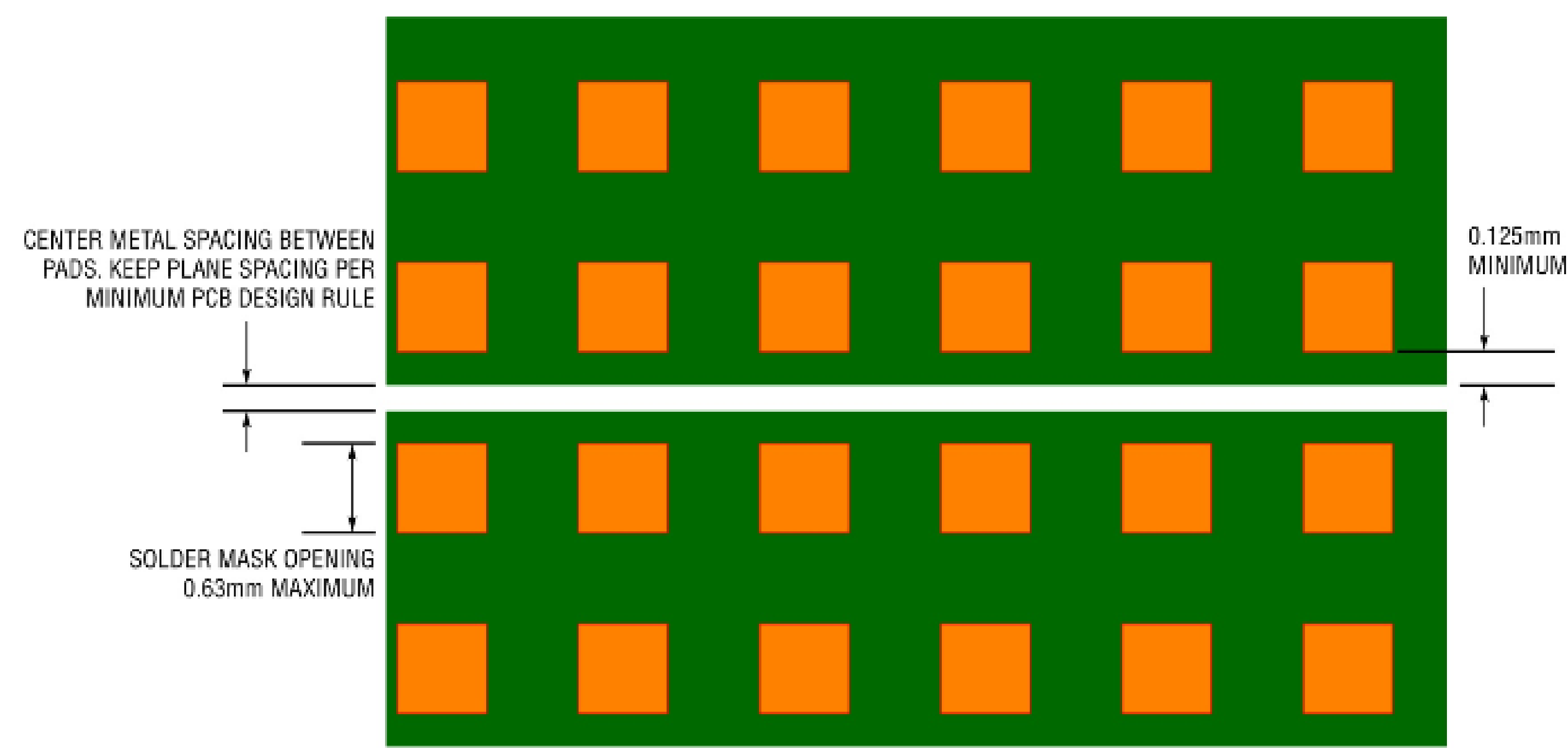
SOLDER MASK ON BT

BT

Thermal relief is used by some customers on the power/ground planes. Customers need to ensure that the resulting thermal relief topology does not cause solder balling within the vias.

PCB Plane Separation

Maximum solder mask opening for plane separation needs to be controlled;
Stencil opening in this area can be reduced to 0.6 to ensure no bridging;
Critical area – under Inductor and plane separation



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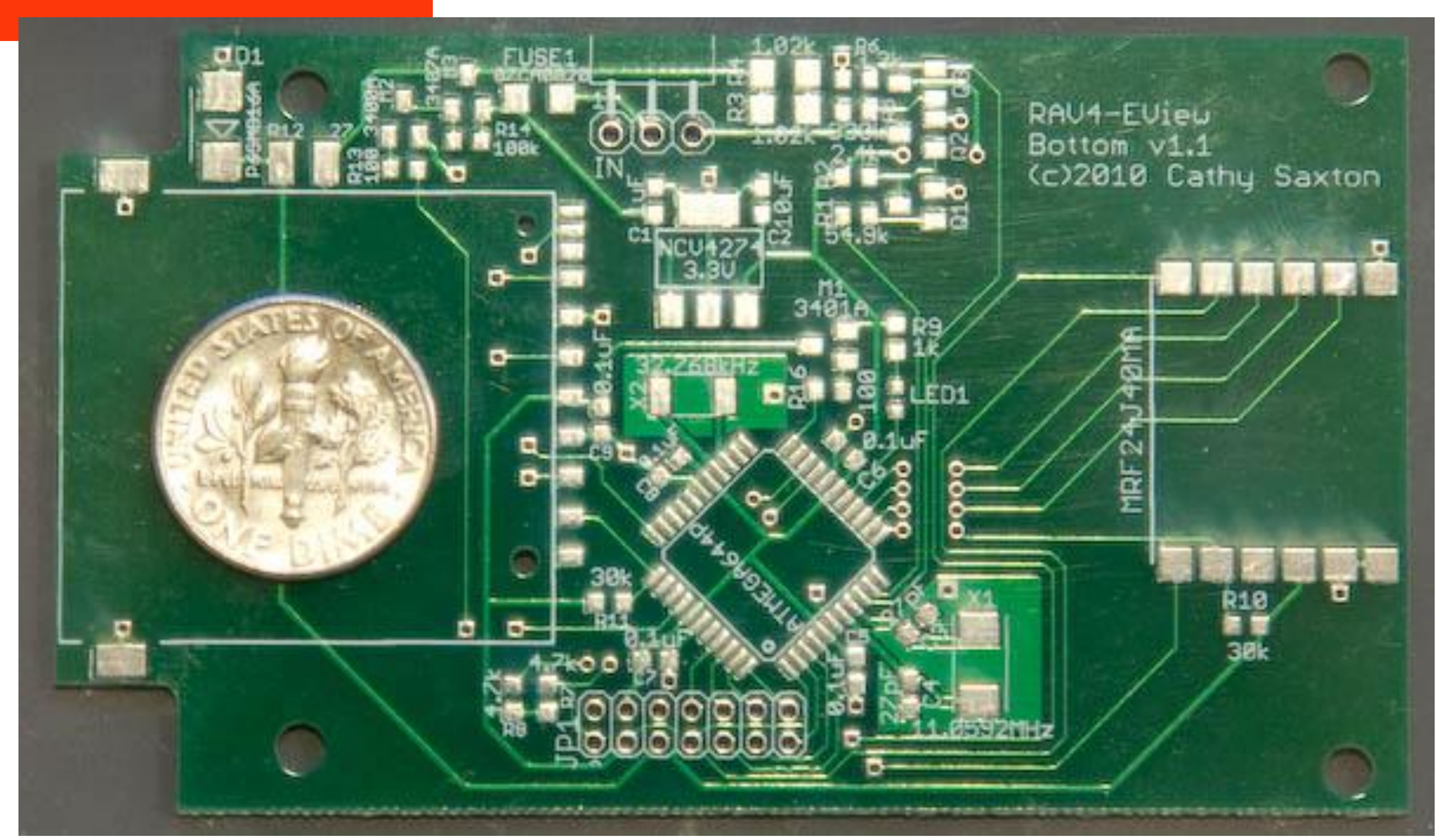
Stencil Design Recommendation

- Stainless steel laser cut stencils recommended
- Recommended stencil thickness 0.125 mm (5 mils) to 0.15 mm (6 mils)
  - Recommend slightly smaller stencil aperture than the pad opening (especially for SMD pads)
    - Stencil Opening 0.605 to 0.62 mm
    - To prevent paste from contacting solder mask
  - Solder volume ~0.05 mm^3 / Pad
  - 4 mil thick stencil not recommended (due to low stand off)
  - Corner radius of 0.06 mm on the aperture recommended
- Stencil area ratio (W/ 4*t) > 0.66 (not an issue for this aperture size)

  where W = Pad width, t = Stencil thickness

Laser solder paste stencil

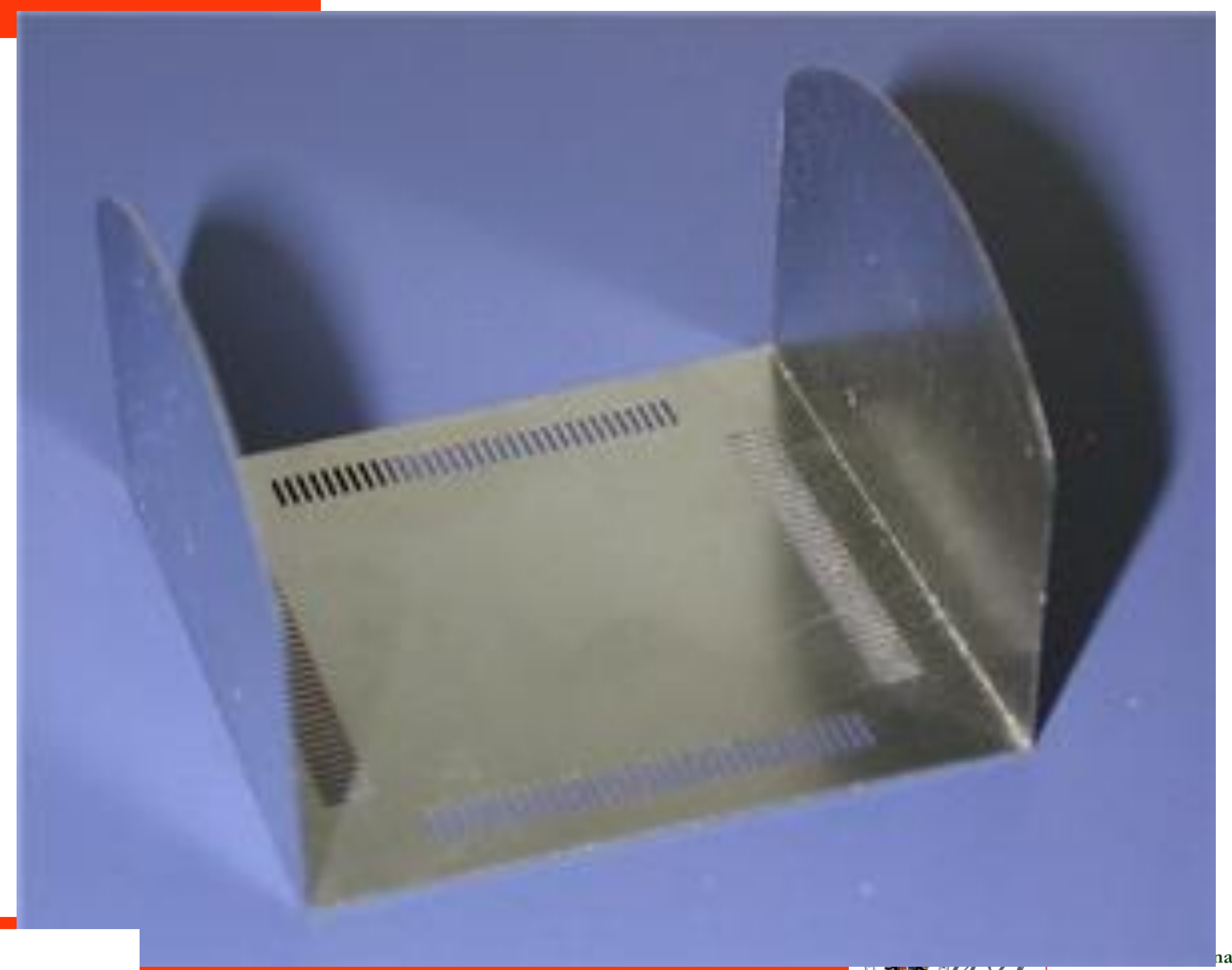


Using solder paste stencil

URL

Mylar solder paste stencil

Hand solder paste stencil



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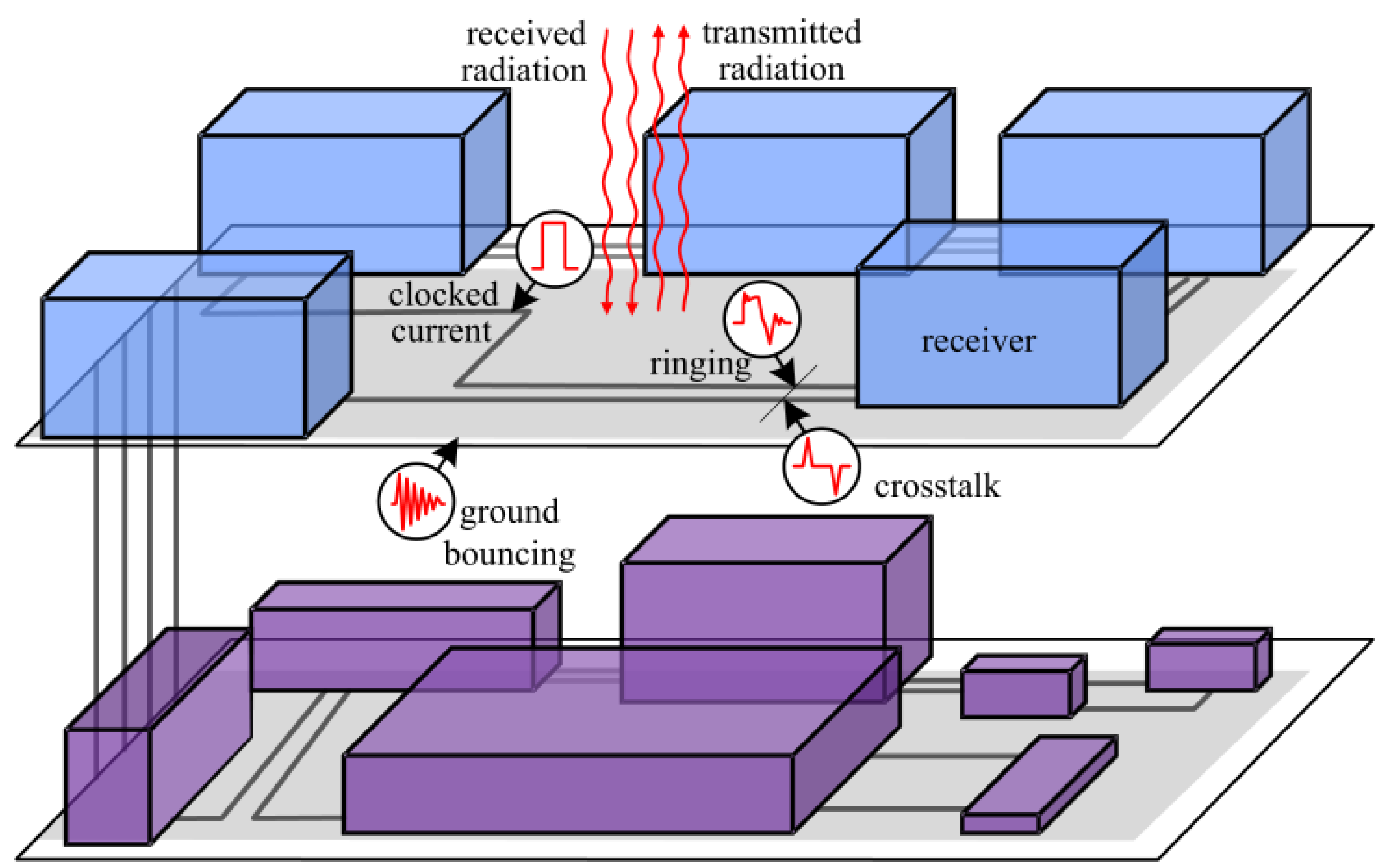
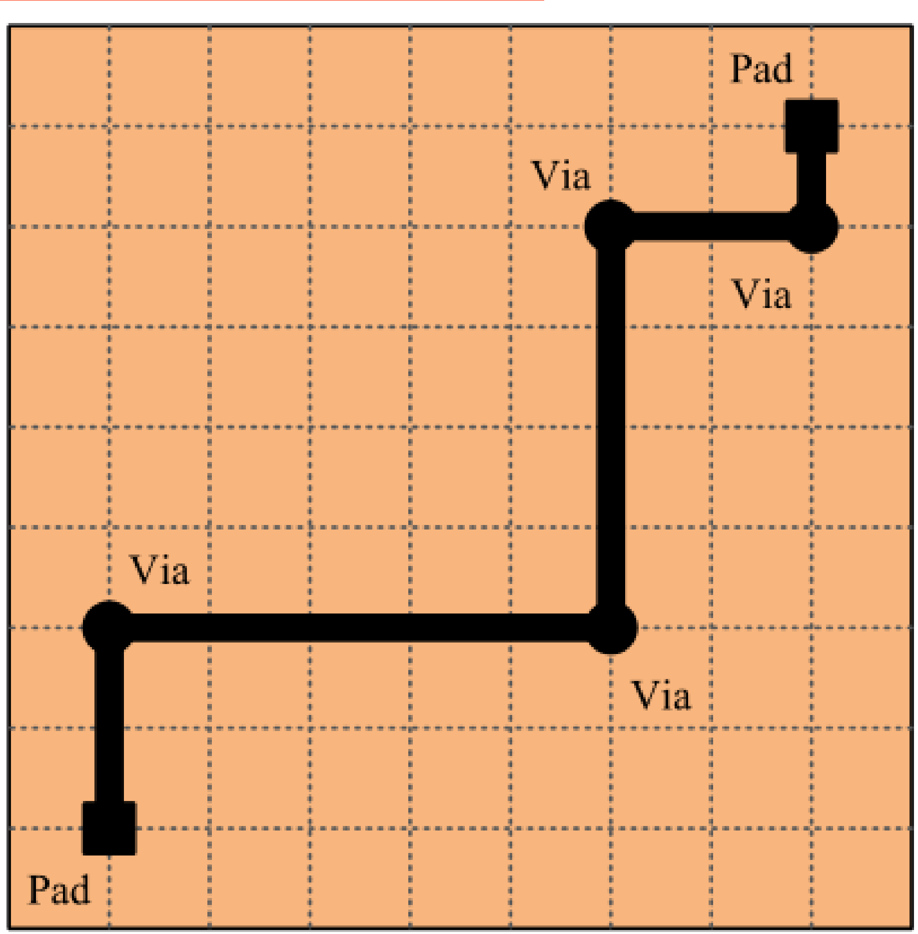
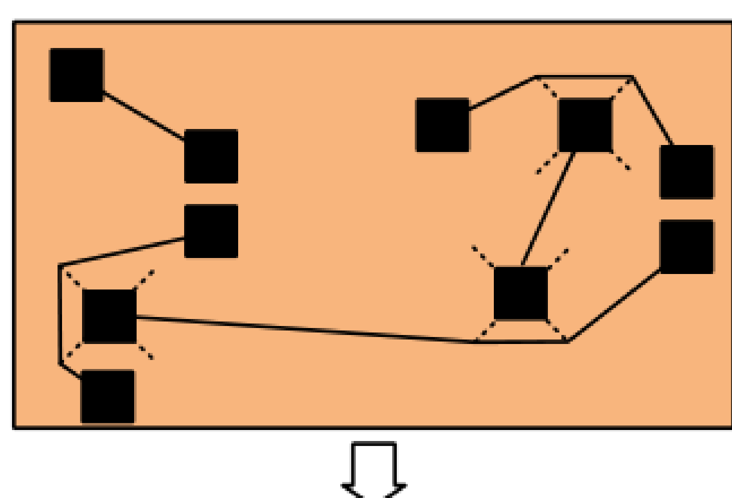
Signal Integrity

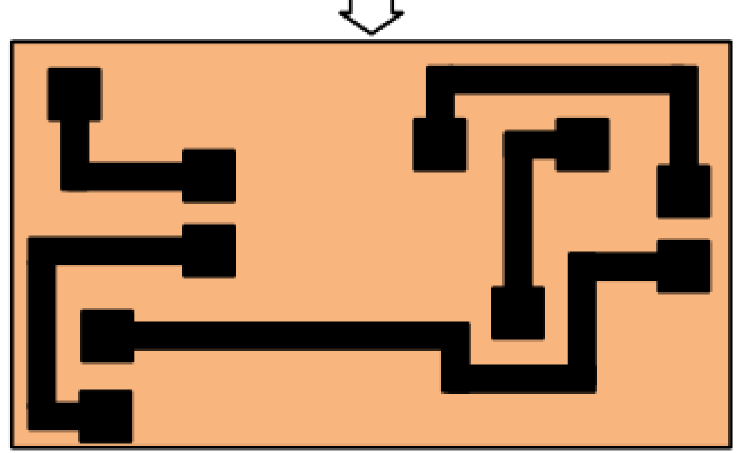


Routing



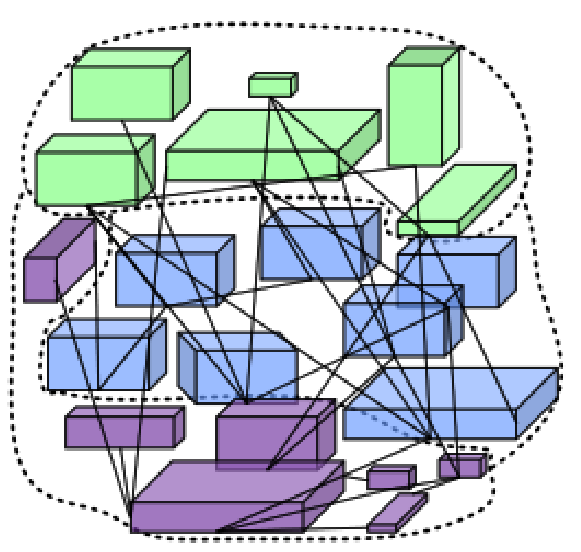
a) 4-Via-Routing



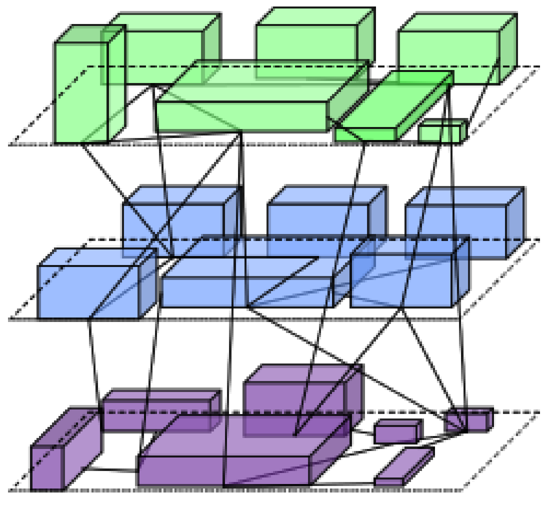


b) Rubber Band Routing

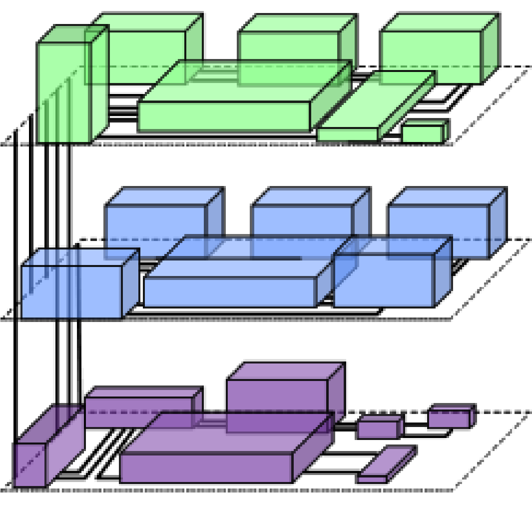
Determination of Component Arrangements



a) Partitioning



b) Placement



c) Routing

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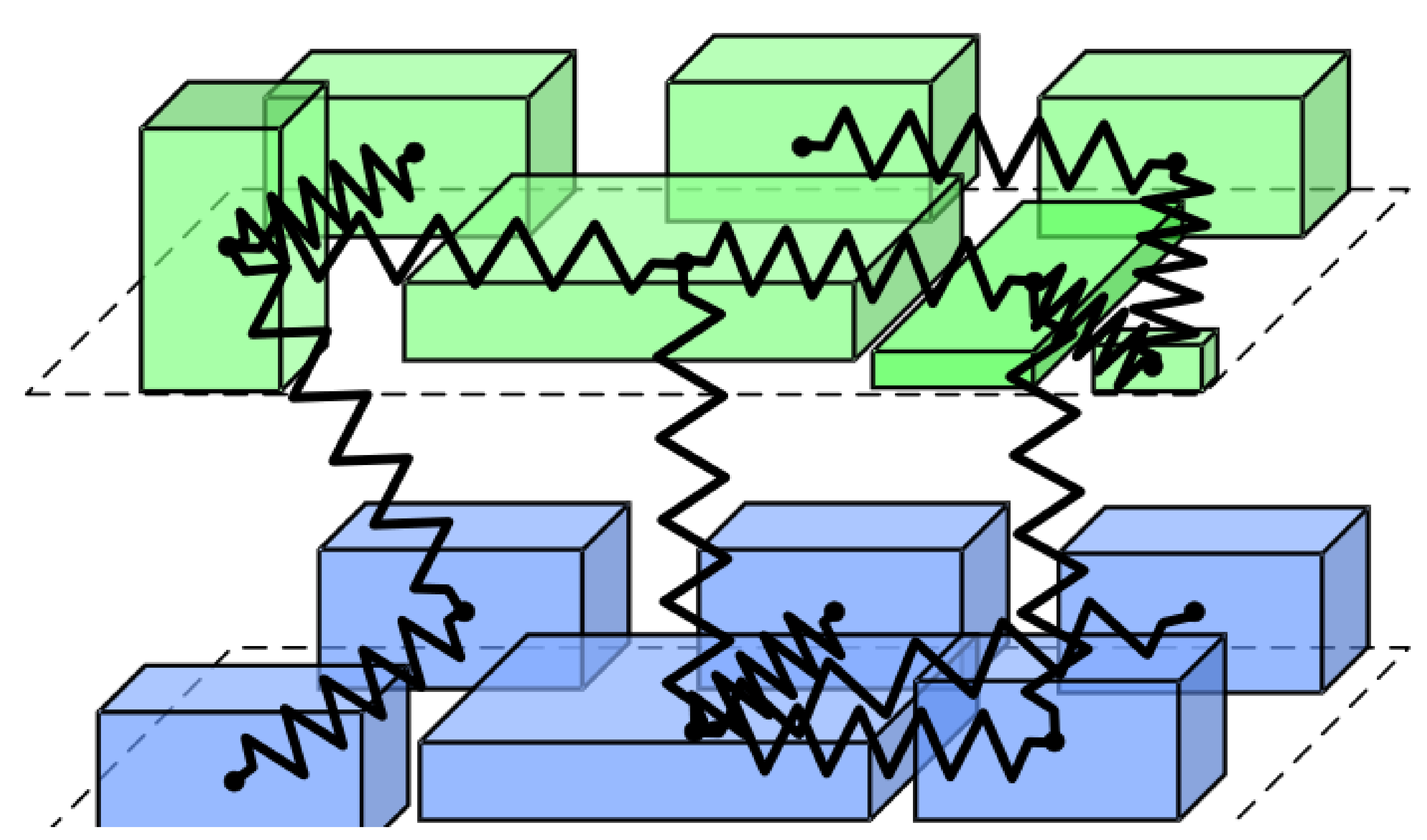
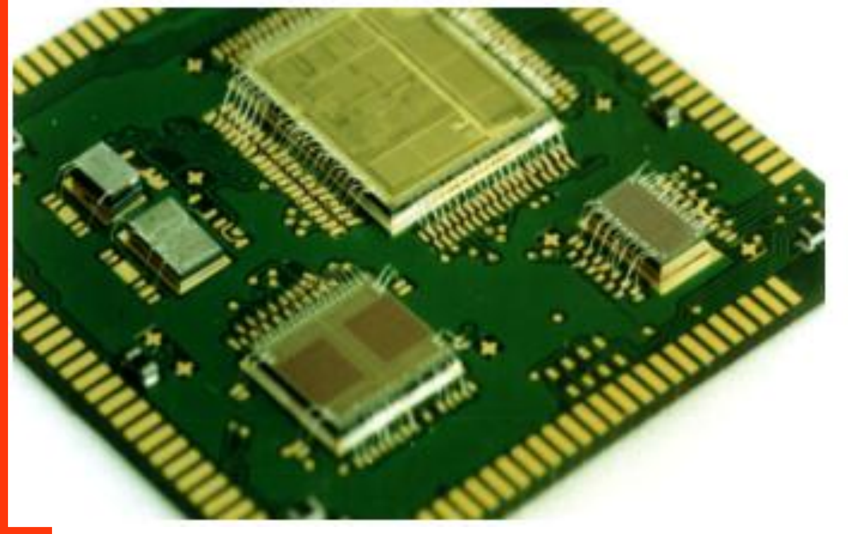
Force Directed Placing

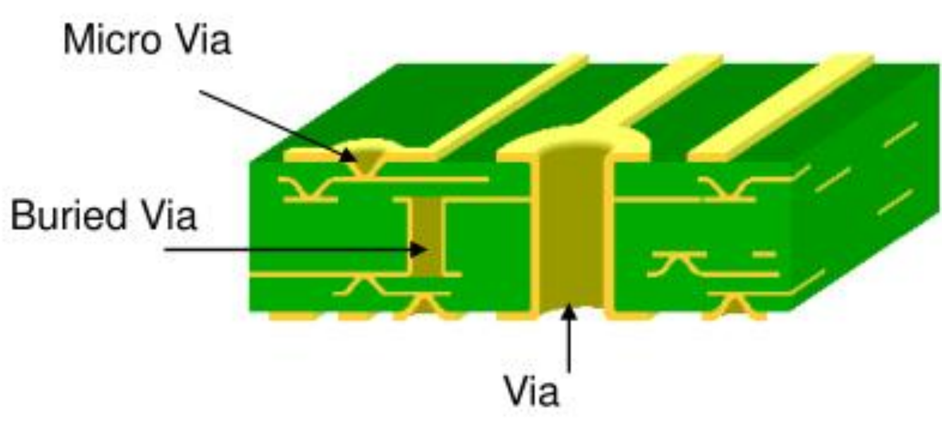


Substrate Technologies – Laminates

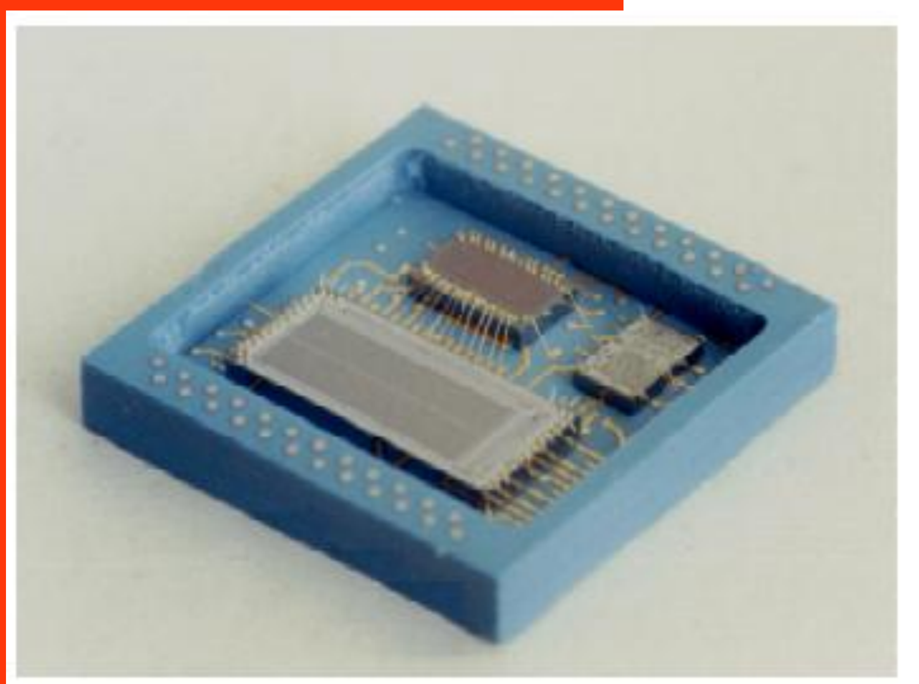
Characteristics:

	HDI	Standard PCB
Material:	Epoxy glass / FR4	
Dielectric constant:	2,3 – 4,7	4,7
Line width / pitch:	75 / 75µm	125 / 125 µm
Via diameter:	100µm	650µm
Layers:	8 – 10	8 - 30
CTE:	14 – 18 ppm	
Thermal dissipation:	poor, medium	
Costs:	medium	low



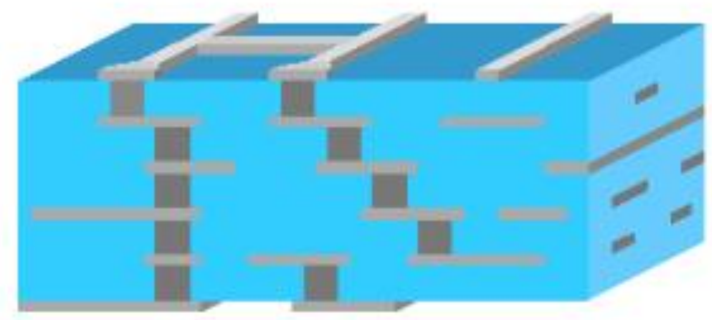


Substrate Technologies – Ceramics

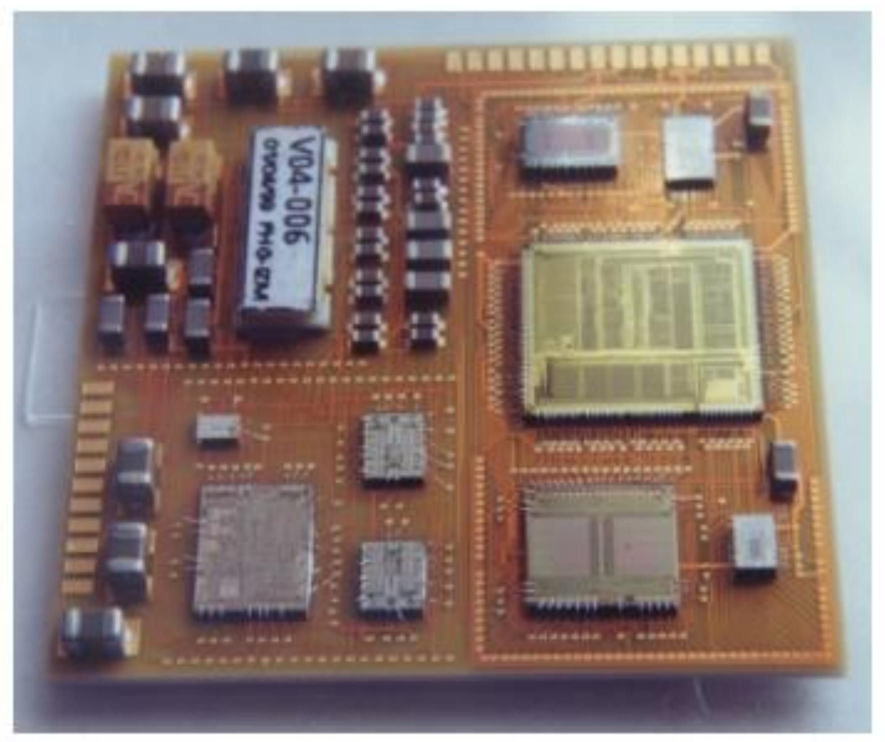


Characteristics:

Material:	Al_2O_3, Glass ceramics
Dielectric constant:	6 – 10
Line width / pitch:	125 / 250 µm
Via diameter:	200 µm
Layers:	15 – 30
CTE:	7,9 – 10 ppm
Thermal dissipation:	high
Substrate costs:	moderate

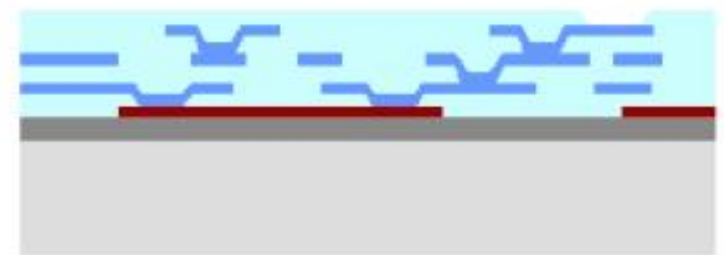


Substrate Technologies – Thin Film



Characteristics:

Material:	Si, Polymers
Dielectric constant:	2,7 – 3,5
Line width / pitch:	10 / 10 µm
Via diameter:	30 µm
Layers:	2 – 5
CTE (Si)	2,6 ppm
Thermal dissipation:	high
Substrate costs:	moderate, high



Area versus Packaging Types

ℓ_c

$1.2\ \ell_c$

$1.5\ \ell_c$

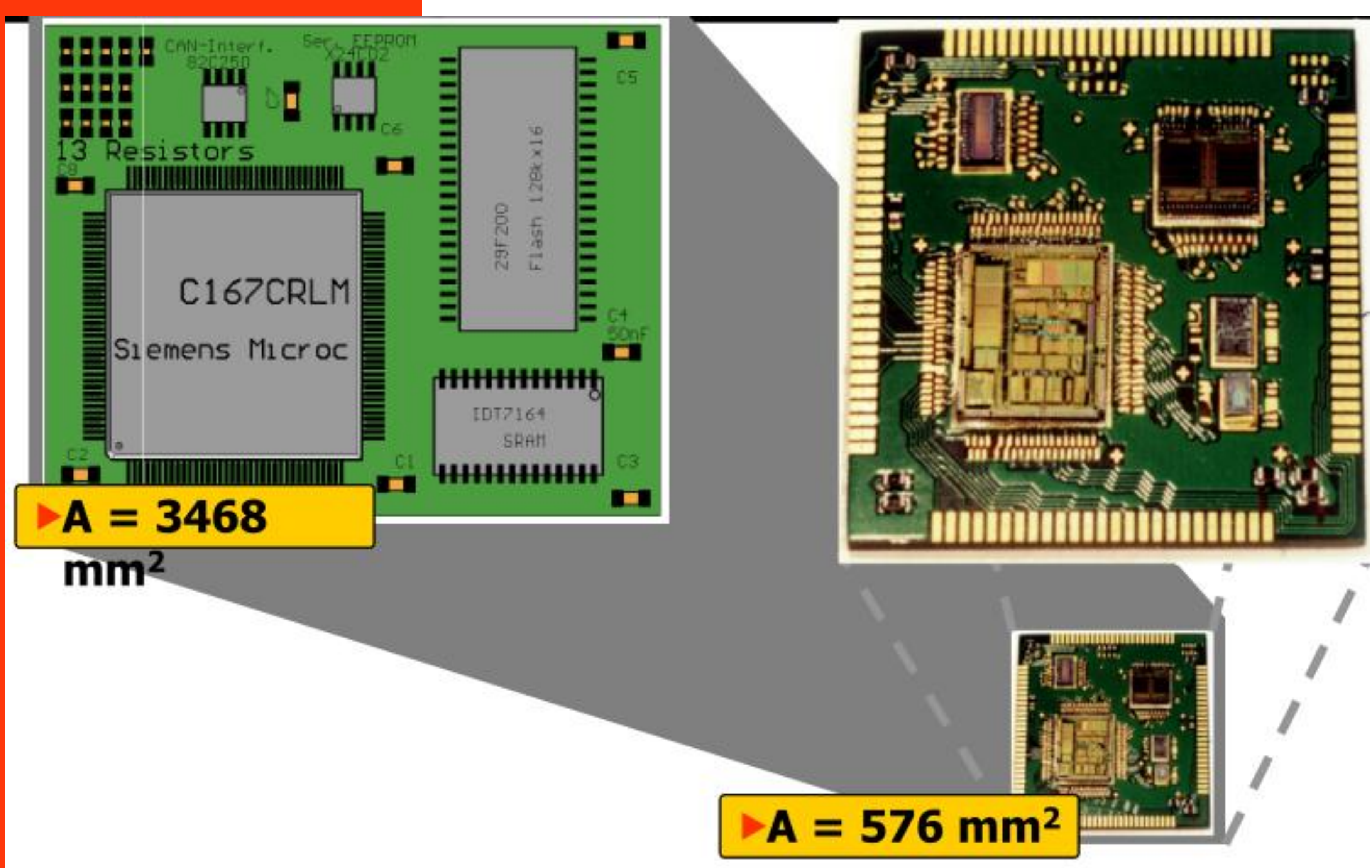
$2.0\ \ell_c$

$3.0\ \ell_c$

Technology	Area ratio package/chip
Flip chip	1:1
Chip-scale package	1.5:1
Chip-on-board	2.5:1
Tape automated bonding	4.0:1
Quad flat package	9.0:1

Source: R. Tummala: Fundamentals of Microsystem Packaging, McGraw-Hill 2001

Miniaturization by Novel Assembly Technologies / Directassembly



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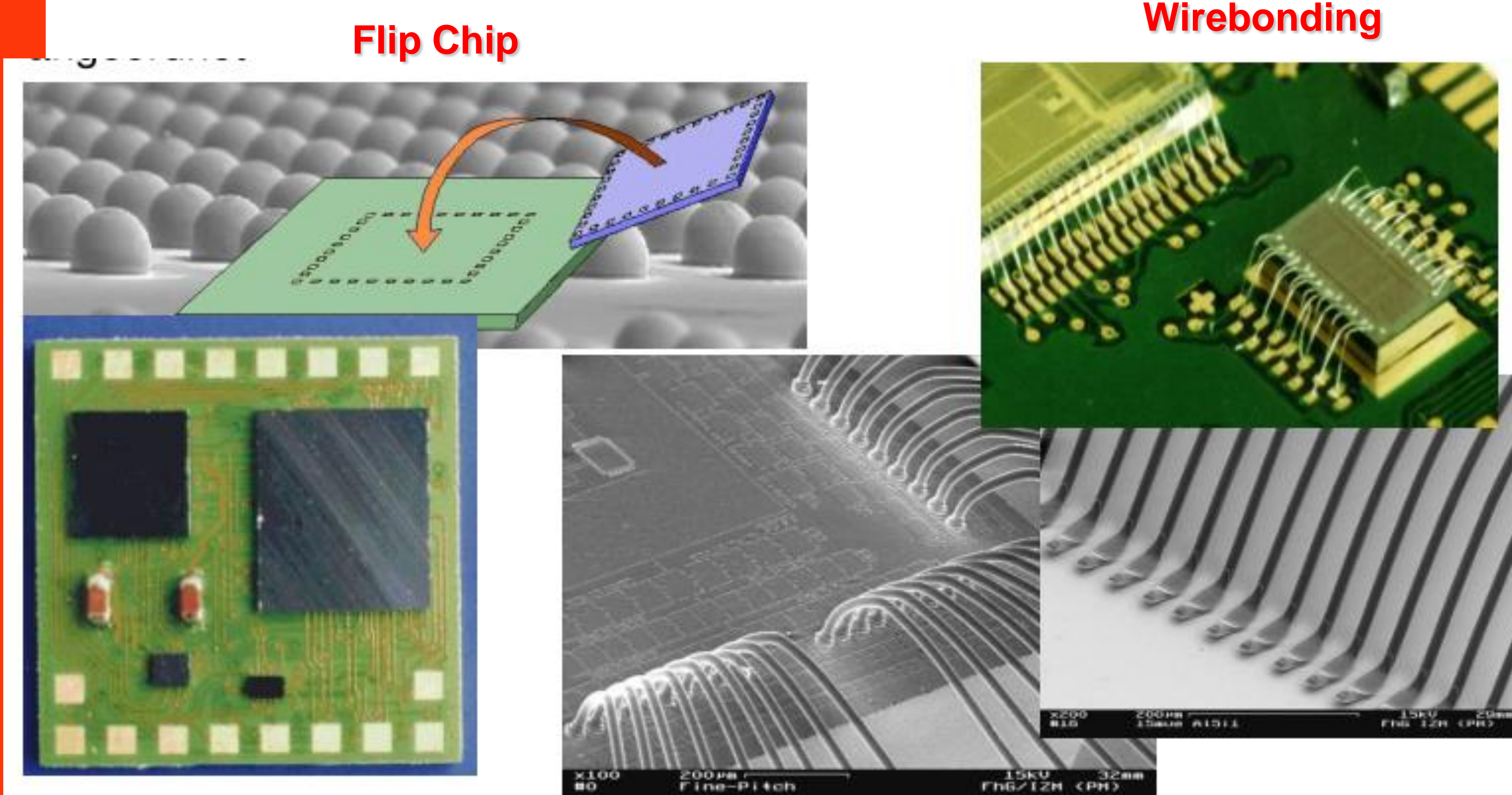
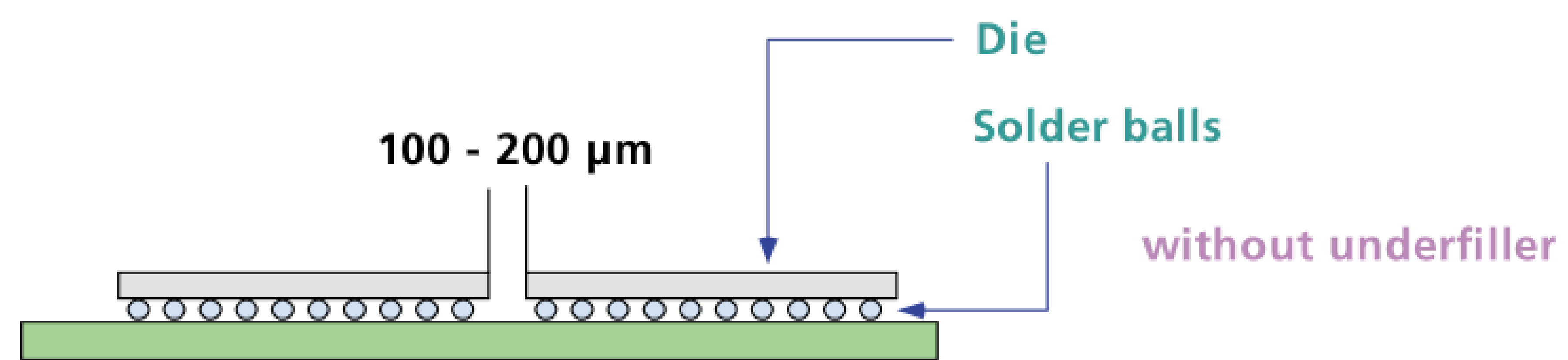
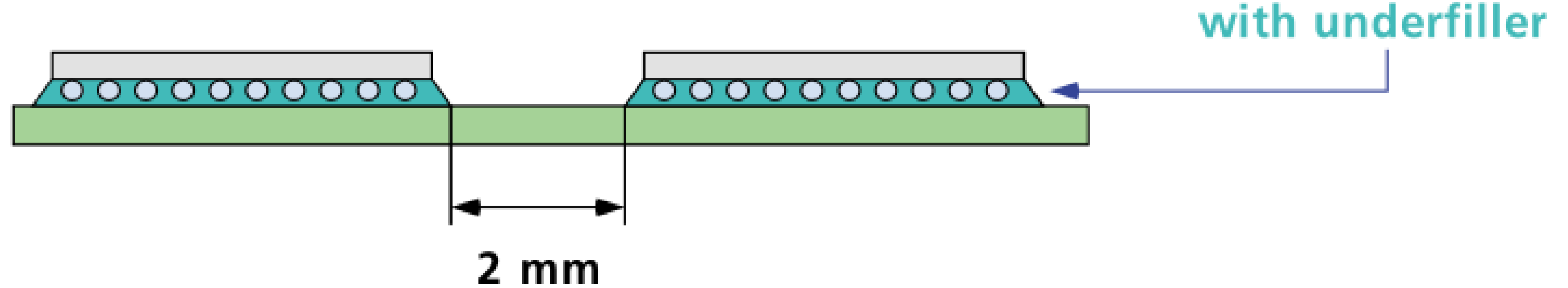
Miniaturization by
Novel Assembly Technologies / Directassembly



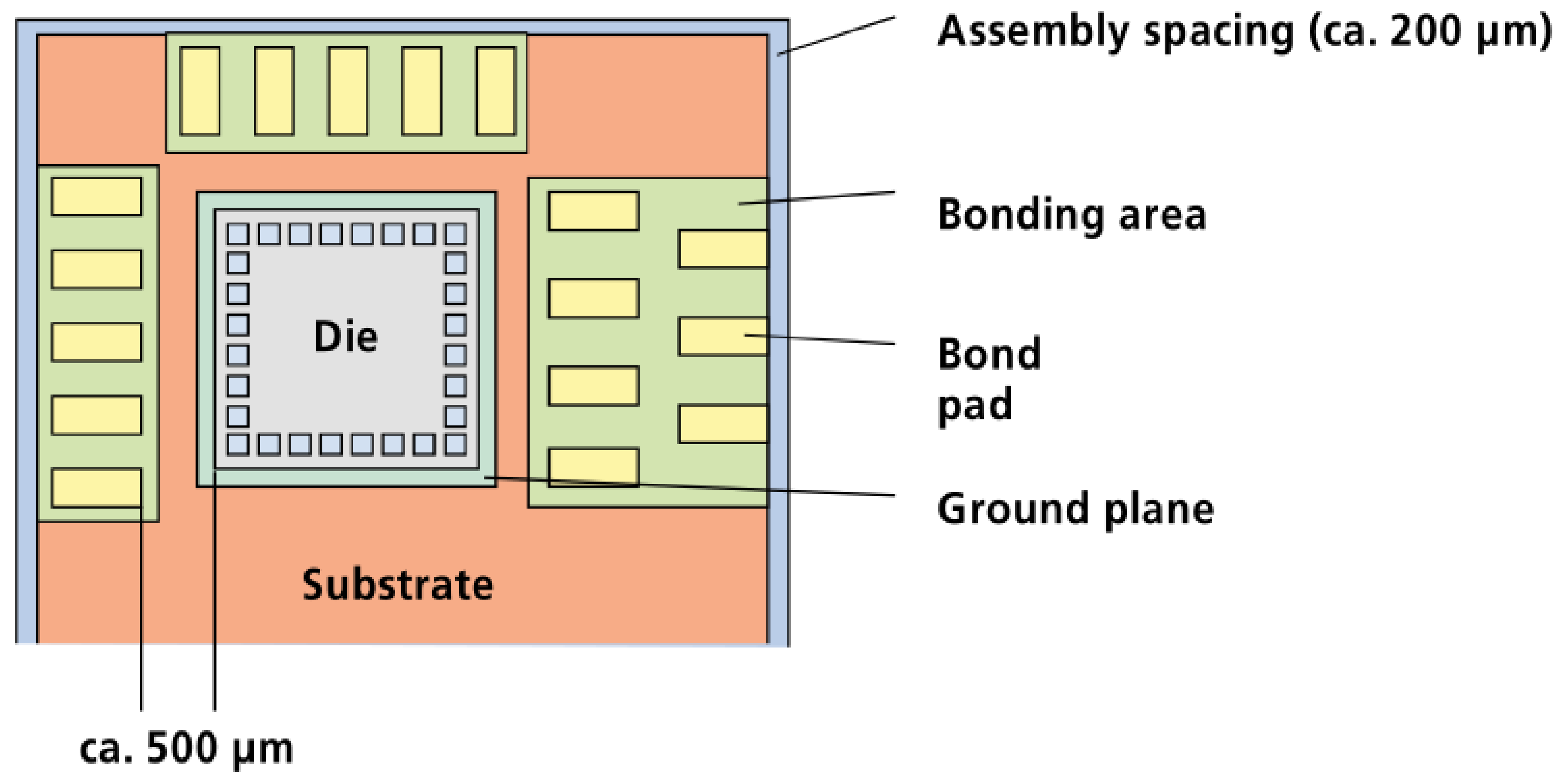
Footprint – Wire Bonding versus Flip Chip

Footprint of Flip Chip – Contact

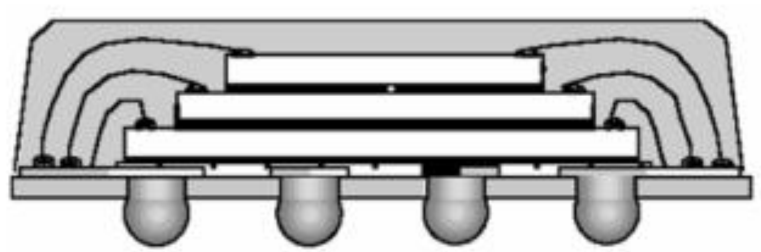


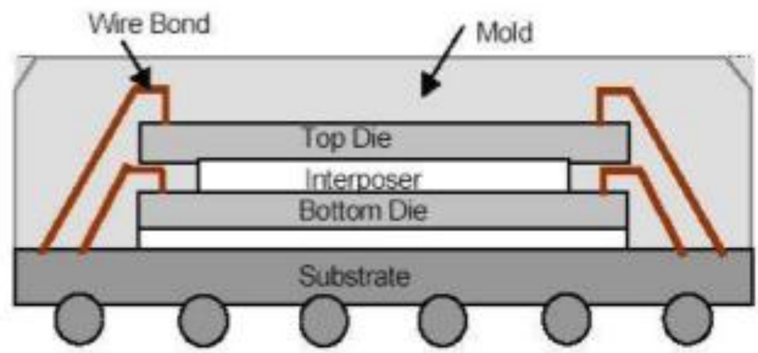


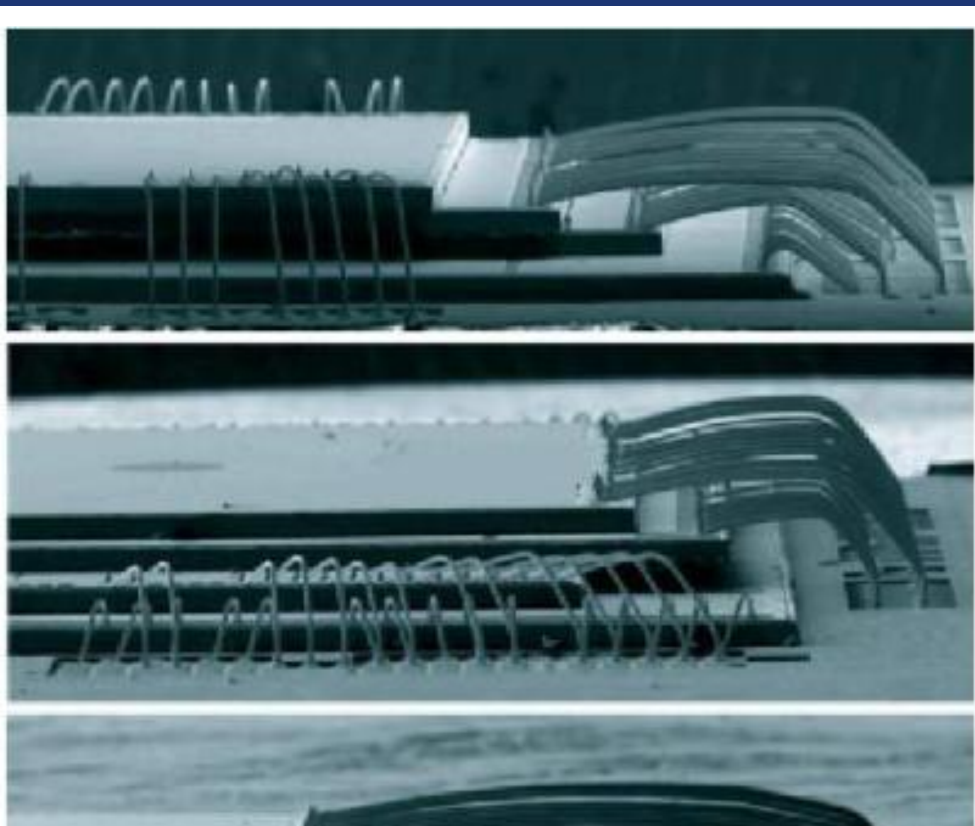
Footprint of Wire Bonding – Contact



High Packing Density by 3-D Packaging





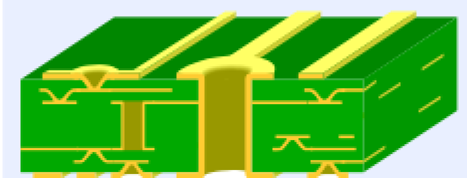


Source: Klossner, Babinetz, Semicon 2002

Source: Sharp

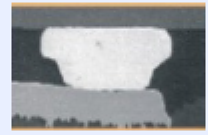
Roundup of the Technology – Parameters

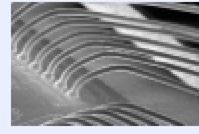
Substrate



	MCM-L HDI	MCM-L Standard PCB	MCM-C Ceramics	MCM-D Thinfilm
Line width [µm]	75	125	125	10
Line space [µm]	75	125	250	10
Via land ø [µm]	100	650	200	30
no. layers	8…10	8…30	15..30	2..5
Dielectrics	Epoxy	Epoxy	Alumina	BCB/PBO
Diel.const.	2,3…4,7	4,7	6…10	2,7…3,5
Base material	FR4	FR4	Alumina	silicon, metal
Price (4 layers)	medium	Low (cents/cm²)	medium	High ($/cm²)

Interconnects





		Wire Bond	Flip Chip	TAB
Min pad pitch [µm]	*Die*	50	120	60
	Substr.	120	120	200
Mounting		serial (2-10 bonds/sec)	parallel	serial/parallel
Electr. Performance	*L [nH]*	1-5	0,06-0,2	1-3
	C [pF]	0,2-0,6	0,02-0,03	0,2-0,6
Mechanical Protection		glob top	underfill	none

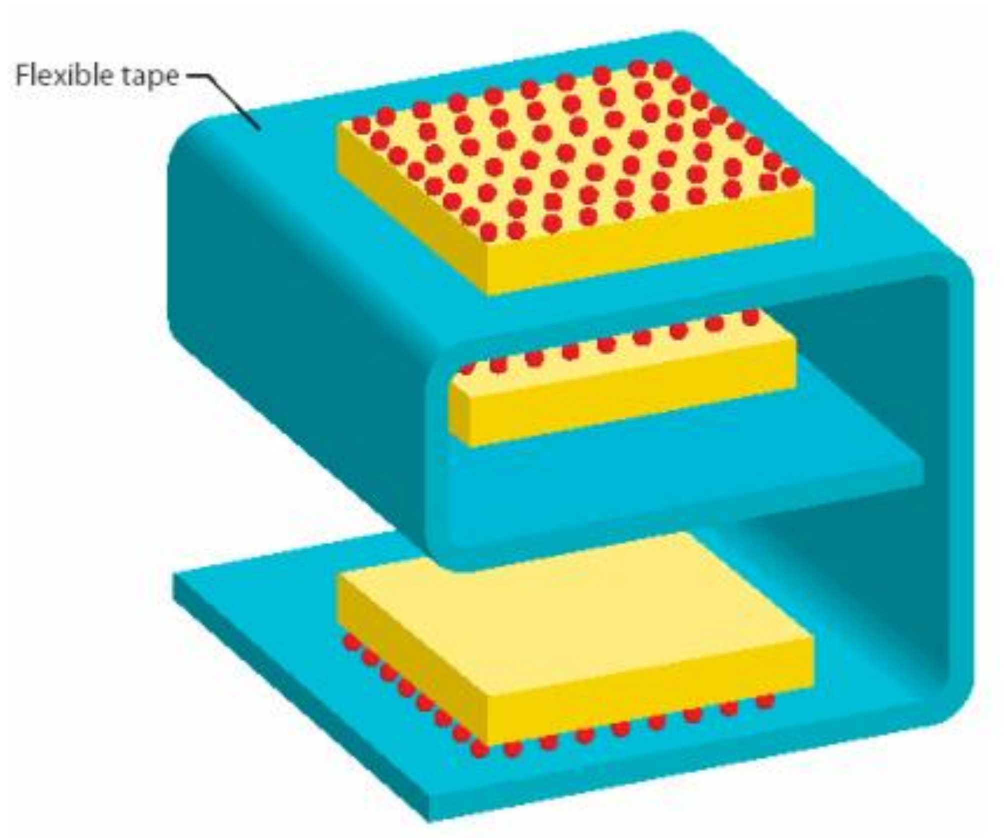
D. Polityko
FSP Mikroperipherik, TU Berlin

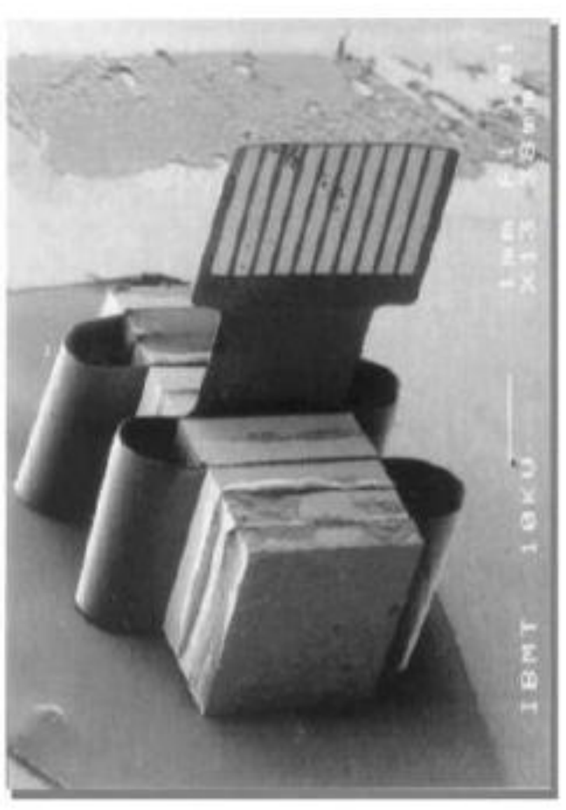
Wire Bounding Example

Gold wire bonding - Video-1

Wire bonding - Video-2

High Packing Density by 3-D Packaging





Source: J. Balde, Foldable Flex And Thinned Silicon Multichip Packaging Technology

Example for the layout of a wiring bearer

Soldering Stop
(Solder resist layer)

Metallization in order to preserve solderability (e.g. Tin)

Buried via

Fiber/Epoxy Laminate

Prepreg-Laminat

Copper Foil

V_{Supply} -Layer

Ground-Layer

Signal-Layers

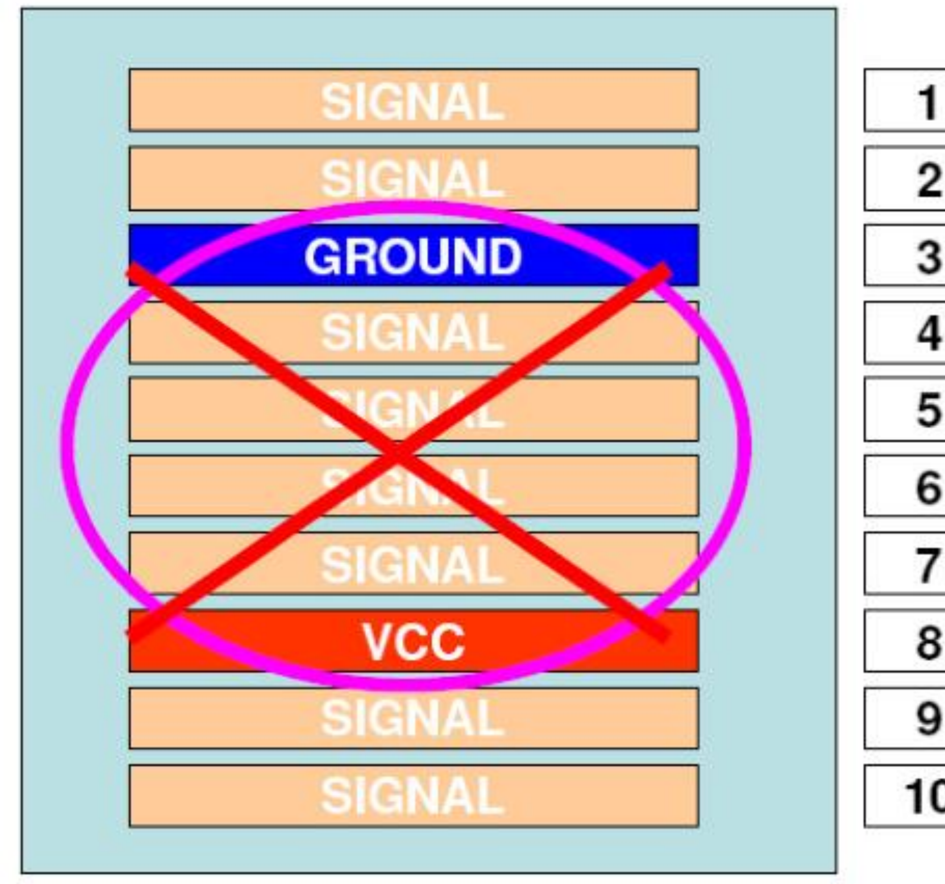
Via sidewalls, metallized with chopper

Blind via

Via (Through-hole)

R. Tummala: Fundamentals of Microsystem Packaging, McGraw-Hill 2001

Layer Layout for the High Speed Design



Layer	
1	SIGNAL
2	GROUND
3	SIGNAL
4	SIGNAL
5	VCC
6	GROUND
7	SIGNAL
8	SIGNAL
9	GROUND
10	SIGNAL

Signal Integrity

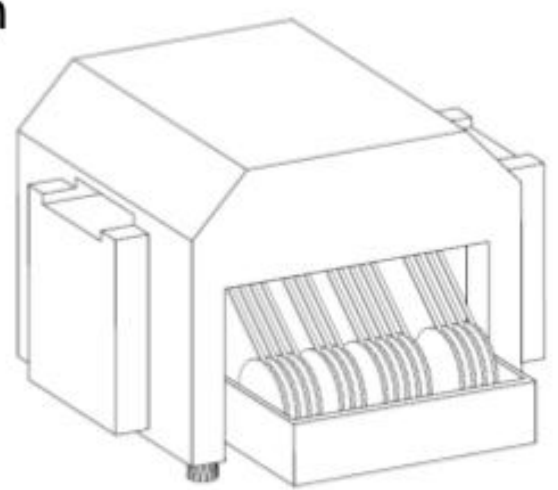
Multifunctional Block
Memory
RF/
Analogue Die
Int.
Antenne
SiP
PCB
Embed. Passives
Digital Block
SMD
1
3
1
3
2
1
4

Determination of Process Costs

Fabrication scenario	Process flow	Process parameter
Products (PD): 1 Product	1. Substrate insert	**Setup (T_0):** 5-30 min / LOT
Fabrication lot (LOT): 1 lot per PD	2. Dispense solder	**Process time (T):** 1 min / FU
Fabrication units (FU): 1000 Units per LOT	3. Place SMDs	**Process capacity (k_E):** 1
Devices (DEV): 25 Devices per FU	4. Reflow	**Material costs (c_{DT}):** $0.002/CON
Contacts (CON): 100 Contacts per FU	5. Deflux	**Tooling costs (c_{DT}):** $250/PD
	6. Test	**Operator hourly rate (C_{Lh}):** $12/h;
		Equipment hourly rate (C_{Eh}): $12.50€/h
		Defect rate (Y_P): 100ppm/CON

Typical Data relevant for cost determination

- SMDs
  - Equipment $50,000 ...180,000
  - Setup 5 ... 30 min per component and lot
  - Process time 0.03 ... 6s per component
  - Yield = 100 ... 20.000 ppm per component
- Bare dies
  - Equipment $300,000
  - Setup 5 ... 30 min per component and lot
  - Process time 1 ... 30s per component
  - Yield = 100 ... 20.000 ppm pro Komponente
  - Tool costs: $150€ per wire-bonded IC;
    upto $20,000 for back-side-assemblye



Determination of Substrate Costs

Substrate technology	Substrate material	Line pitch [µm]	Via diameter [µm]	Metal layer maximal	Embedded passives	Embedded dies
Standard-PWB	FR4	250	125	12	-	-
SBU Substrate	FR4	100	75	8	+	+
Laminated Flex	PI	100	75	4	+	-
Ceramic substrate	Al2O3	200	125	2	+	-
Thinfilm substrate	Al2O3	20	20	4	+	+

Process step	Process time [h]	Equipment cost [k$]	Material cost [$/inch²]	Operator utilization	...
Insert laminate	0	0	0.021	1	
Clean laminate	0.25	50,000	0.003	1	
Punch tooling holes	0.5	0	0	1	
Drill entry & exist materials	0	0	0.002	1	
Drill through holes	0.0025	300,000	0.001	0.5	
Deburr holes	1.2	80,000	0	1	
Desmear through holes	0.6	125,000	0.001	1	
Electroless plate through holes	0.6	500,000	0.002	1	
Apply resist to laminate	5	90,000	0.004	1	
Insert art work	0	0	0.0003	1	
Artwork registration	1	60,000	0	1	
Expose	0.5	60,000	0	1	
:	:	:	:	:	
Screen & dry legend	2	80,000	0.001	1	
Fabrication	0.5	500,000	0	1	
Automatic optical inspection	1	500,000	0	1	

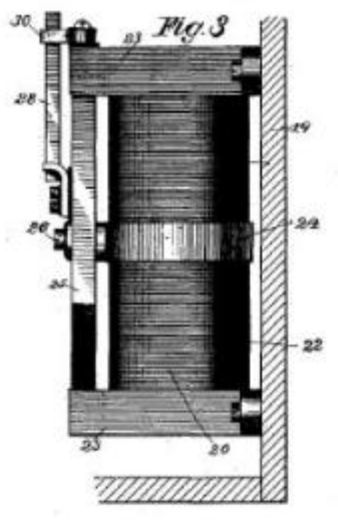
Assembly Technologies

MCM: Multi Chip Module (MCM) is an electronic system or subsystem with two or more bare integrated circuits (bare die) or Chip Sized Packages (CSP) assembled on a substrate

BCB
Cu
Flip-Chip
Au/Ni/Cu
Wire-bonding
L
R
C
Passivation
signal-2
signal-1
4-Layer PWB-4 PCB Substrate
Buried vias
BGA balls
Blind vias
Solder mask

Assembly Technologies

VCM: Voice Coil Motor. The incumbent actuator technology for miniature AF cameras is the voice coil motor.
VCMs are named as such because they are based on the principles of attraction and repulsion between magnets to generate sound from electricity. The technology was first patented in 1874



VCM : is the incumbent technology used ina miniature camera to move a lens module and alter focus.
The technology, shown in an 1888 patent by Alex. Graham Bell (**left**), is not fundamentally different from the VCM in a HTC OneX+ smartphone (**right**)

Determination of Assembly Costs

Assembly technology	Substrate	Interconnects	3D packaging
SMM: Standard SMT	Printed wiring board	THT/SMT	-
MCM: Variant 1	SBU/Ceramic/Thinfilm	THT/SMT/WB	-
MCM: Variant 2	SBU/Ceramic/Thinfilm	THT/SMT/WB/FC	-
VCM: Folded modules	Laminated/Thinfilm-Flex	THT/SMT/WB/FC	Substrate folding
VCM: Module stack	SBU/Ceramic/Thinfilm	THT/SMT/WB/FC	Solder ball stack

Process step	TP0 [min]	TB0	TP [min]	TB	CE [k$]	ECA	CM [$]	CMB	CT [k$]	CTB	DL	DLB
Auto THT	30	LOT	0.04	DEV	500	1					100	DEV
Manual THT			0.25	DEV							9000	DEV
Dispense solder	30	LOT	1	ASY	50	1	0.002	CON	0.25	PD	100	CON
Place SMT	120	LOT	0.012	DEV	250	1					100	DEV
Place metal FC parts			0.5	DEV	400	1					500	ASY
Reflow			1.5	ASY	100	1					100	ASY
Deflux			3	ASY	120	12	0.085	ASY	0.25	PD		
Dispense adhesive	45	UDL	8	AIC	70	1	0.66	DEV			100	DEV
Place WB dies	60	DEL	0.12	DEV	70	1			0.25			
Place dies (bottom)	15	DEL	0.12	DEV	70	1			30			
Post cure	30	LOT	125	ASY	10	50						
Plasma clean	9	LOT	2.5	ASY	15	5						
Excise patterned adhesive	15	UDE	0.17	DEV	2	1			200	LOT	1000	DEV
Align & tack bond to IC	60	DEV	2	DEV	250	1			150	LOT	100	DEV
Wire bonding	60	DEV	0.002	CON	150	1	0.16	CON			150	CON
Test WB-chips			0.4	DEV								
Repair WB-chips			20	DEV								
Test SMT/THT-devices			0.4	DEV								
Repair SMT/THT-devices			1.5	DEV								

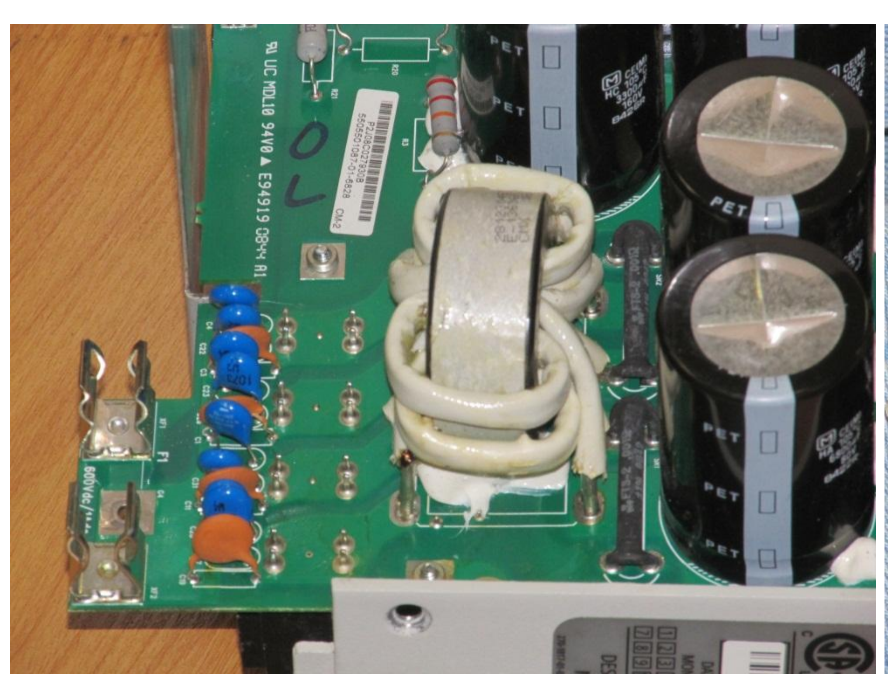
Legend: table caption			
TP	Process time	CM	Material costs
TB	Scale base: proc. time	TB0	Scale base: mat. cots
TP0	Setup time	CT	Tooling costs
TB0	Scale base: setup time	CTB	Scale base: tool. costs
CE	Equipment costs	DL	Defect level
ECA	Equipment capacity	DLB	Scale base: defect level

Legend: scale types			
CON	per contact	AIC	per chip area ["²]
DEV	per device	UDL	p. dev. type & lot
ASY	per assembly	DEL	p. device & lot
PD	per product		
LOT	per lot		
UDE	p. dev. type		

Uso de dos monitores Vista Moderador

http://office.microsoft.com/es-es/powerpoint-help/dar-una-presentacion-en-dos-monitores-mediante-la-vista-moderador-HA010067383.aspx?CTT=5&origin=HP010374495

Control de la energía



Track thickness

The copper in a PCB is rated in **ounces**, and represents the thickness of 1 ounce of copper rolled out to an area of 1 square foot.
For example a PCB that uses 1 oz. copper has a thickness of 1.4mils.

Ounces	Thickness (mil)	Thickness (um)
1/2 oz.	0.7 mil	17.6
1 oz.	1.4 mil	35
2 oz.	2.8 mil	70

Ounces	Min Cu (mil)	Thickness (mil) plated
1 oz.	1.22 mil	2.08 mil (53.248 um)
2 oz.	2.43 mil	3.30 mil (84.48 um)
3 oz.	3.65 mil	4.51 mil (115.456 um)
4 oz.	4.86 mil	5.69 mil (145.664 um)

IPC-2221A "Generic Standards on Printed Circuit Board Design"

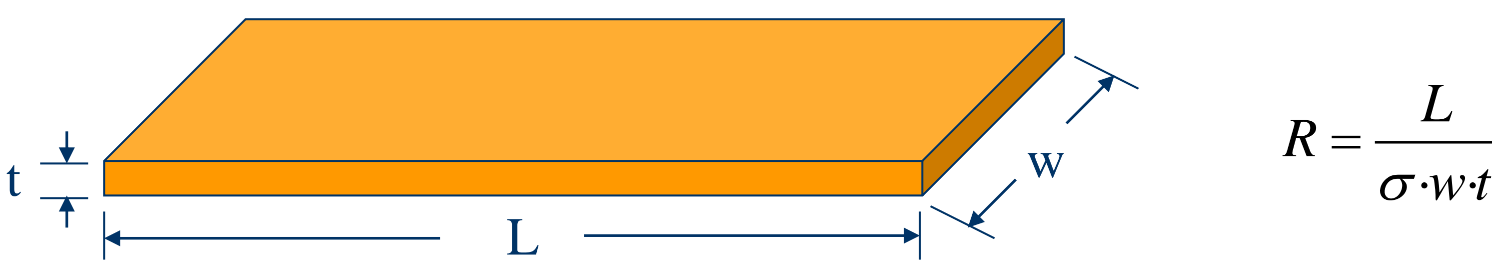
• Calentamiento de las pistas

• La máxima corriente que admite una pista está limitada por el autocalentamiento

$$P = I_{rms}^2 R \quad , \qquad \Delta t = P \cdot R_{th}$$

• Hay que considerar la presencia de elementos calientes cercanos
• Mantener t < 120ºC para FR4
• Regla: - w > 0.3 mm/A, para 1 oz (Δt < 30ºC e
- w > 0.18 mm/A, para 2 oz I < 5 A)
• El “plating” o metalizado puede aumentar el espesor de las pistas en un 40%
• El estañado de las pistas prácticamente no ayuda

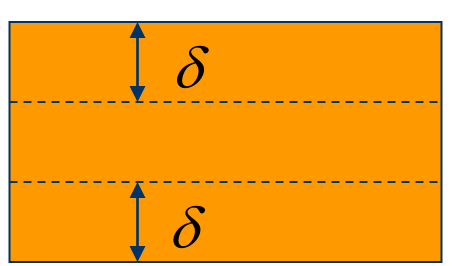
- **Calentamiento de las pistas: Resistencia**



$$R = \frac{L}{\sigma \cdot w \cdot t}$$

$$Cu: \quad \sigma = 5.5 \cdot 10^{7}\ \Omega^{-1} m^{-1} \quad \Rightarrow \quad R = 0.5\ m\Omega \cdot \frac{L}{w} \quad (para\ \ t = 35\ \mu m)$$

- Efecto pelicular:



$$\delta = \sqrt{\frac{2}{\mu\omega\sigma}} \quad . \quad \delta << t \quad \Rightarrow \quad R \approx \frac{L}{\sigma \cdot w \cdot 2\delta}$$

$$f = 1\ MHz \quad \Rightarrow \quad 2\delta = 136\ \mu m$$

$$f = 10\ MHz \quad \Rightarrow \quad 2\delta = 42\ \mu m$$

$$f = 100\ MHz \quad \Rightarrow \quad 2\delta = 14\ \mu m$$

Current Carrying Capability*

$$I = k \cdot \Delta T^{0.44} \cdot A^{0.725} \begin{cases} \Delta T = T_{MAX} - T_{AMBIENT} \quad \text{(Temperature Rise)} \\ k = \begin{cases} 0.048 \text{ for outer layers} \\ 0.024 \text{ for inner layer} \end{cases} \\ A = \text{ Trace cross - sectional area} \end{cases}$$

* IPC-2221A “Generic Standards on Printed Circuit Board Design”

Current Carrying Capability*

Current and Trace Thickness for 1 oz Copper and Maximum allowed Temperature Rise

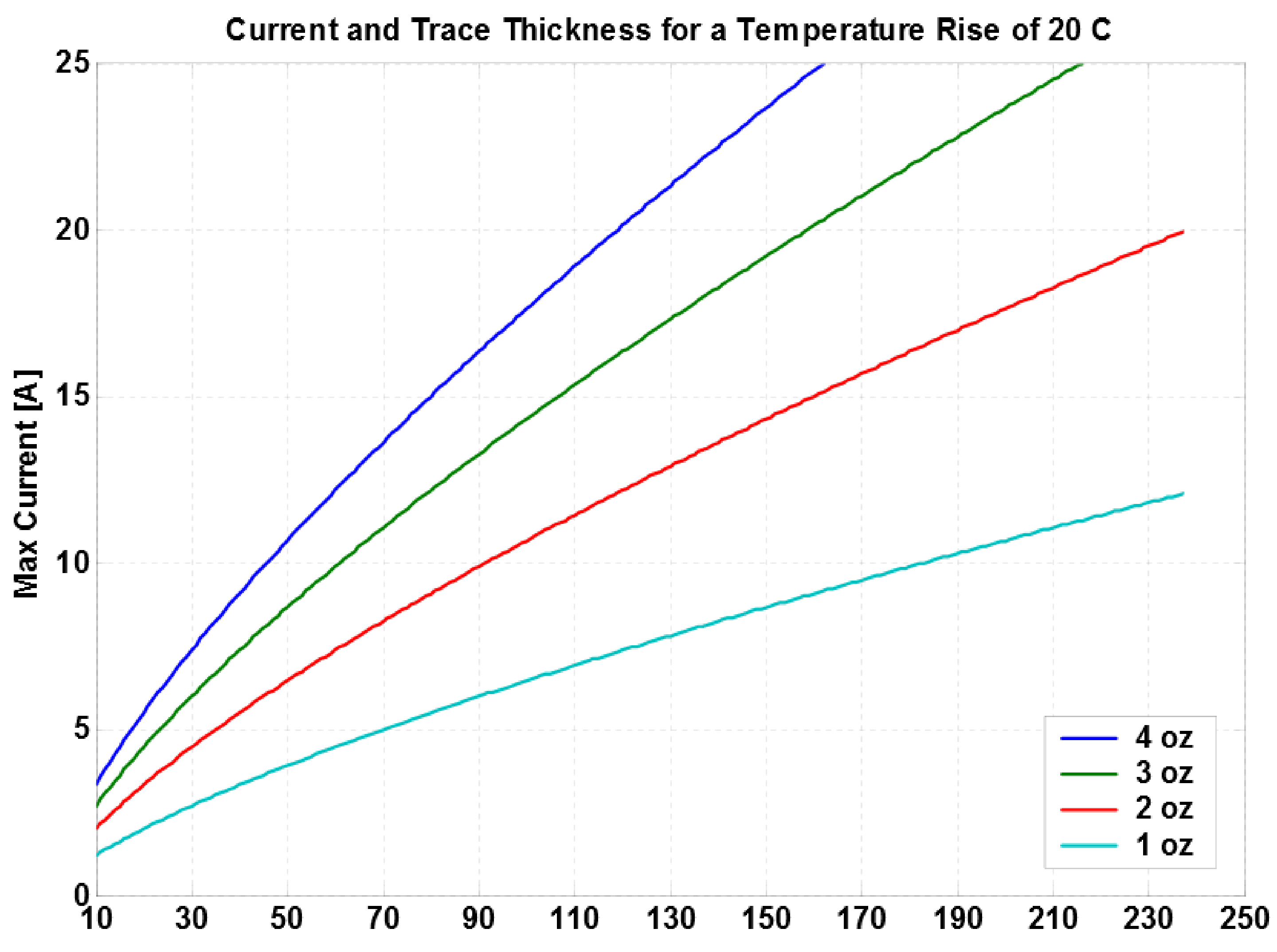
Max Current [A]: 0, 5, 10, 15, 20, 25

Trace Width [mil]: 10, 30, 50, 70, 90, 110, 130, 150, 170, 190, 210, 230, 250

Legend: 100 C, 80 C, 60 C, 40 C, 20 C

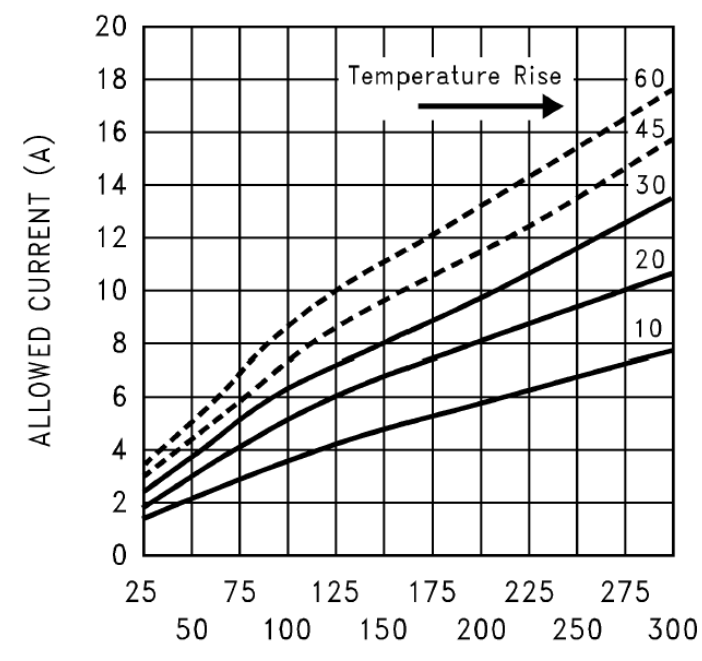
©2004 Robert S. Balog Jr., PE

Current Carrying Capability*



* IPC-2221A “Generic Standards on Printed Circuit Board Design”

- **Calentamiento de las pistas**
  - Un valor práctico: R_{th} = 30ºC/W (cápsula a ambiente)
  - R_{th} mejora con el área, hasta 1” para 1 oz, y unas 3” para 2 oz
  - FR4 es buen conductor térmico ⇒ un plano de Cu en el otro lado ayuda en un 10-20% (hasta un 50-70% con vías térmicas)



Calentamiento de las pistas

Saturn PCB Design, Inc. - PCB Toolkit V6.1 - www.saturnpcb.com

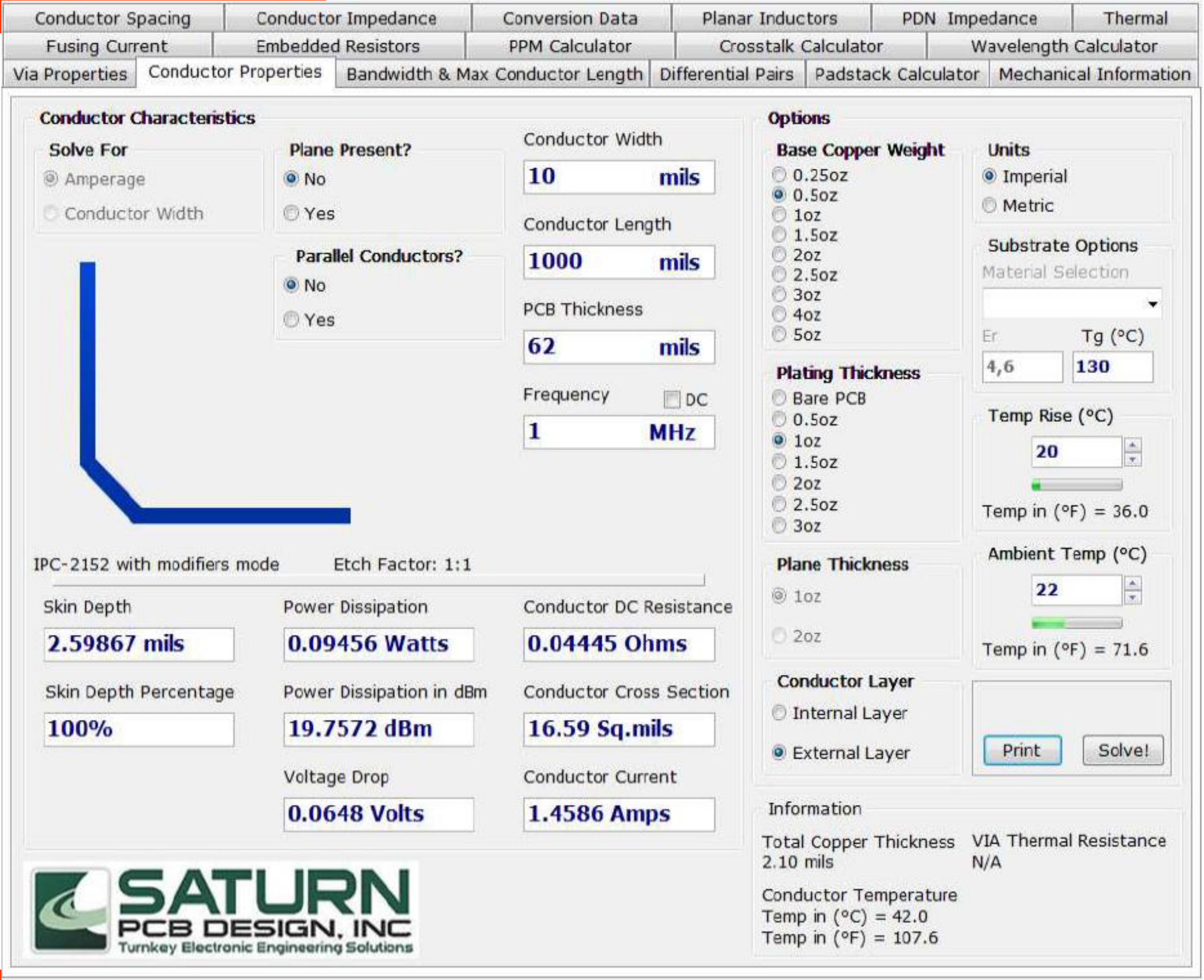
File | Program Function | Tools | Help | Contact Saturn PCB Design, Inc

- Via Properties
- Conductor Properties
- Bandwidth & Max Conductor Length
- Differential Pair Calculator
- Padstack Calculator
- Mechanical Information
- Minimum Conductor Spacing
- Conductor Impedance
- Conversion Calculator
- Planar Inductors
- PDN Impedance
- Thermal Management
- Fusing Current
- Embedded R's
- PPM Calculator
- Crosstalk Calculator
- Wavelength Calculator

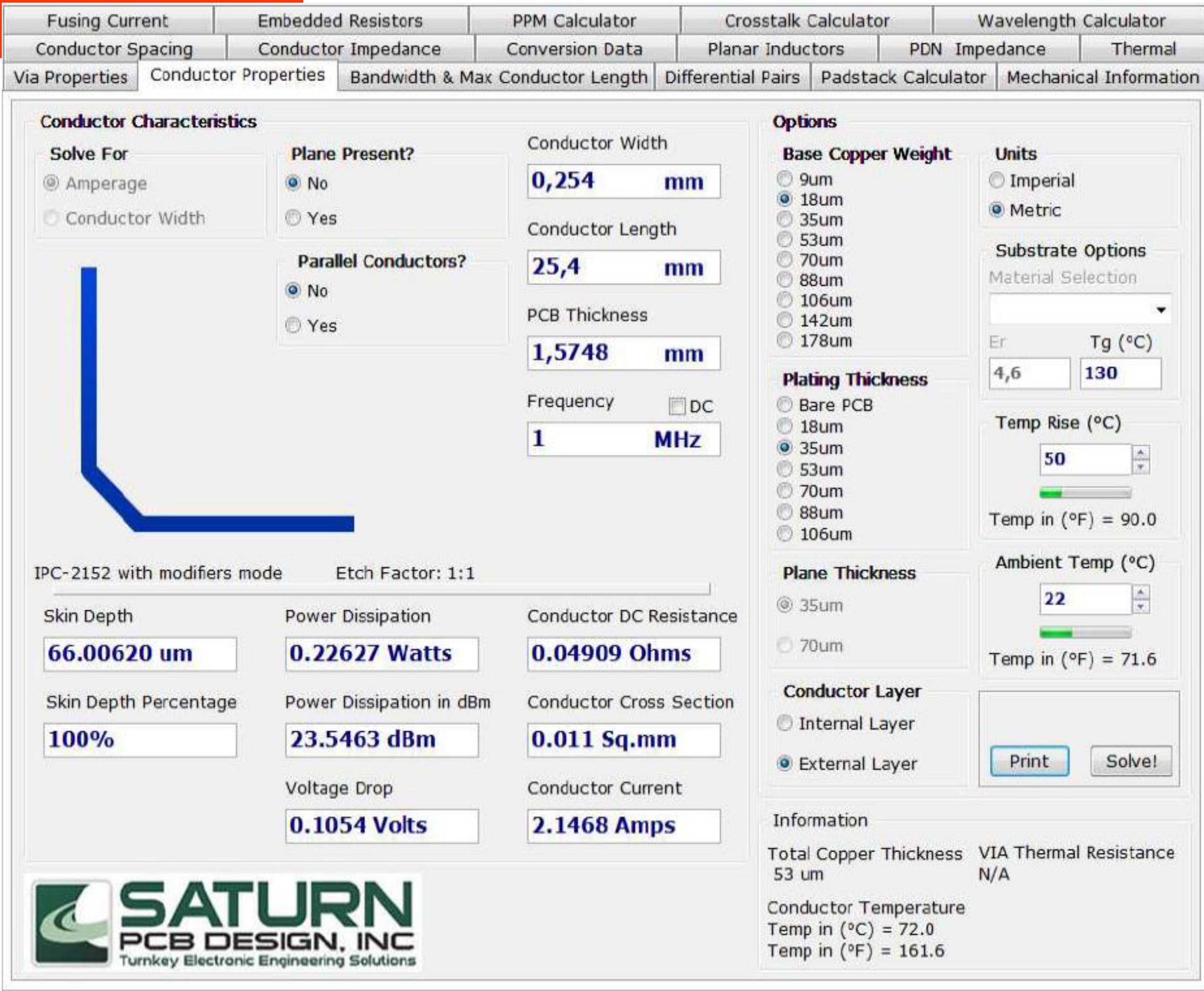
Norma IPC-2152:

"Standard for Determining Current-Carrying Capacity In Printed Board Design"

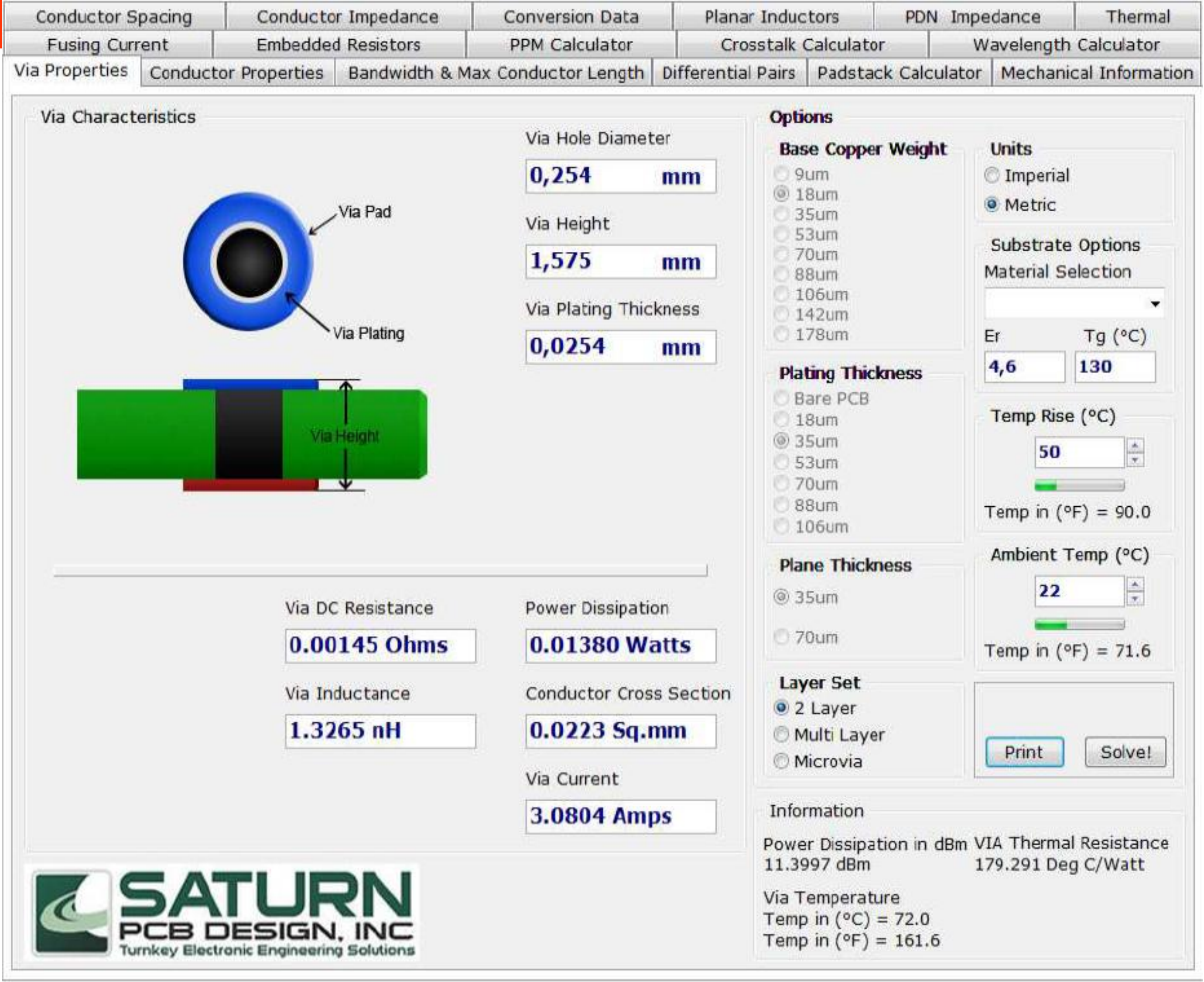
Calentamiento de las pistas



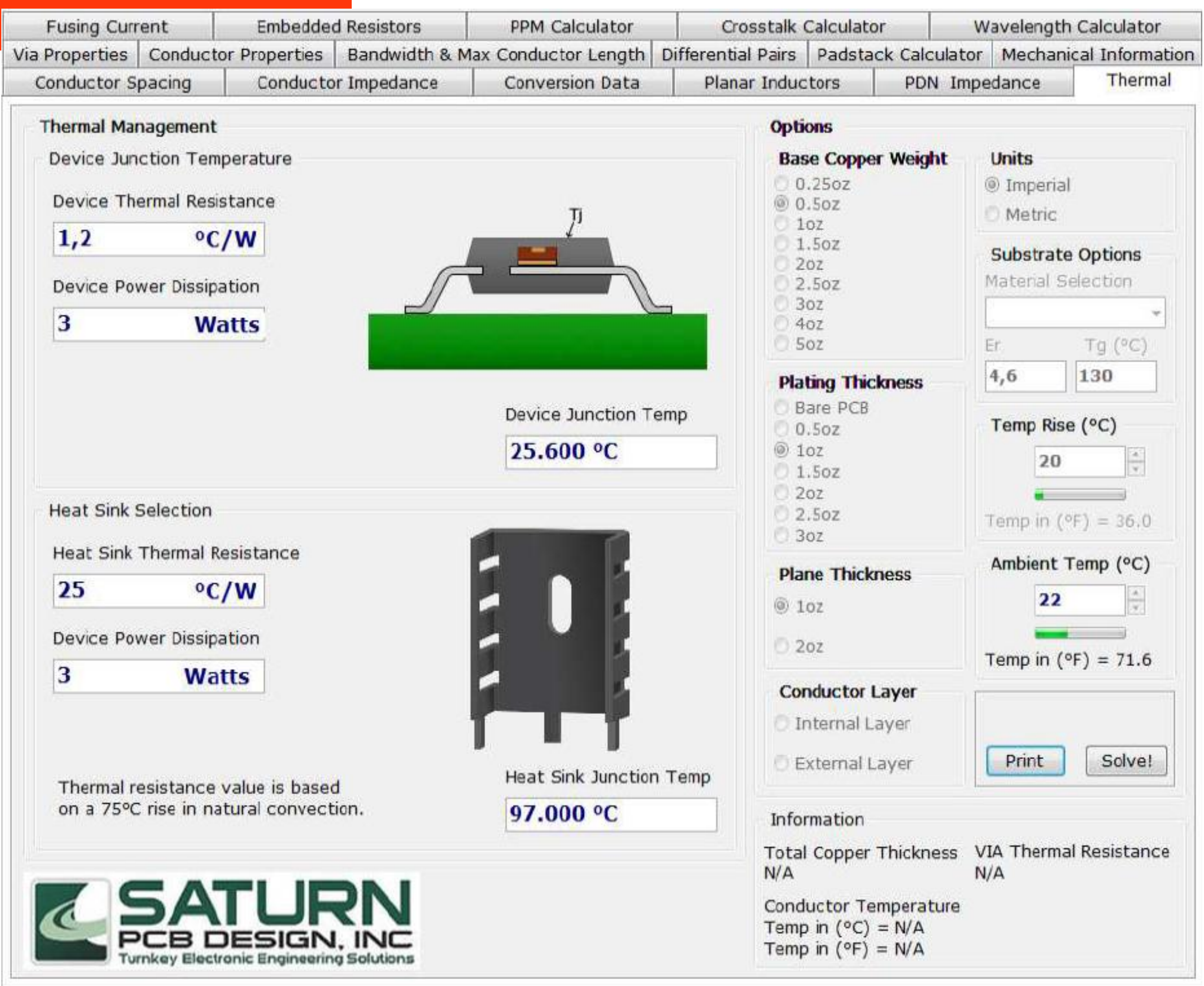
Calentamiento de las pistas



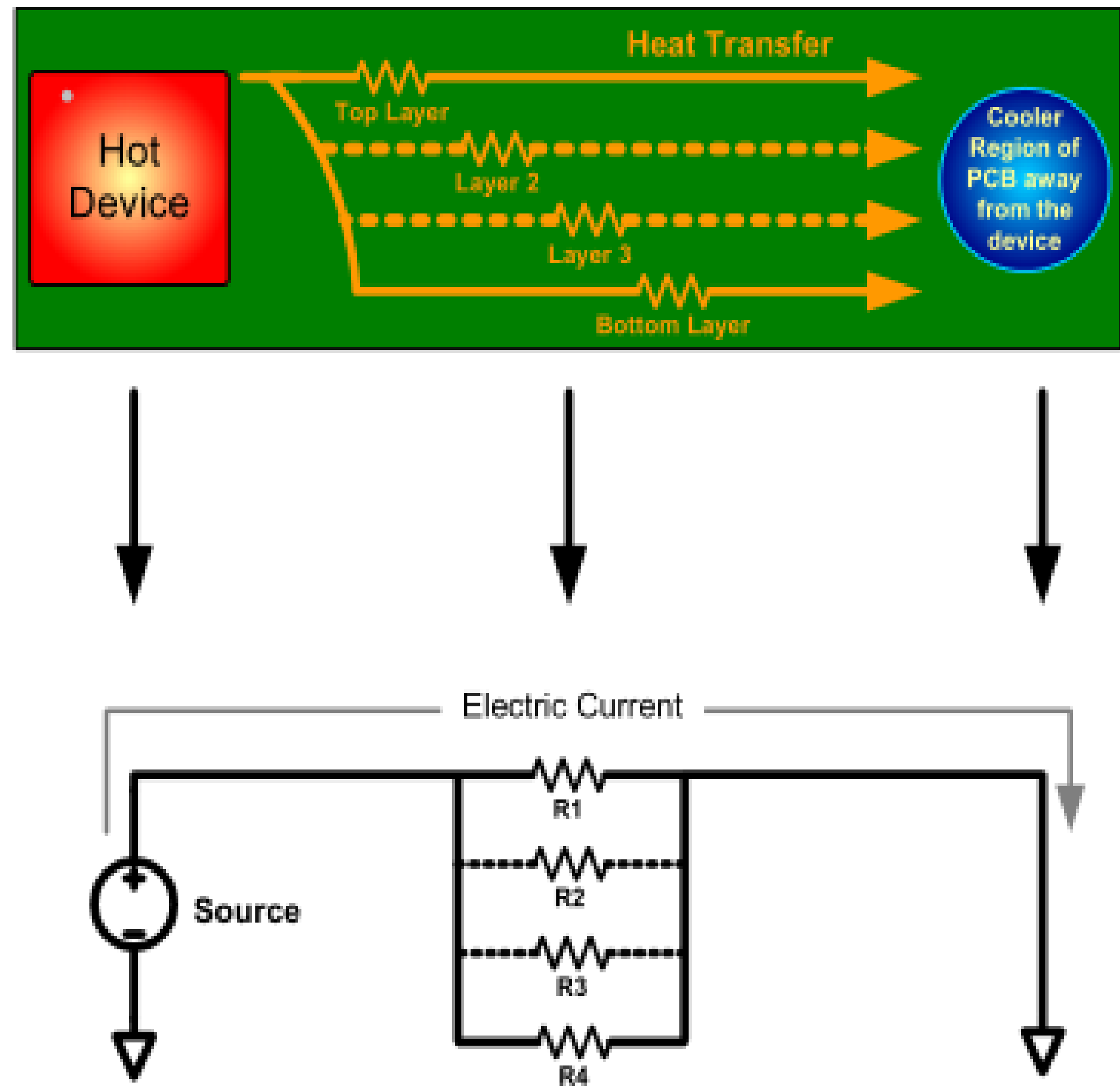
Calentamiento de las pistas



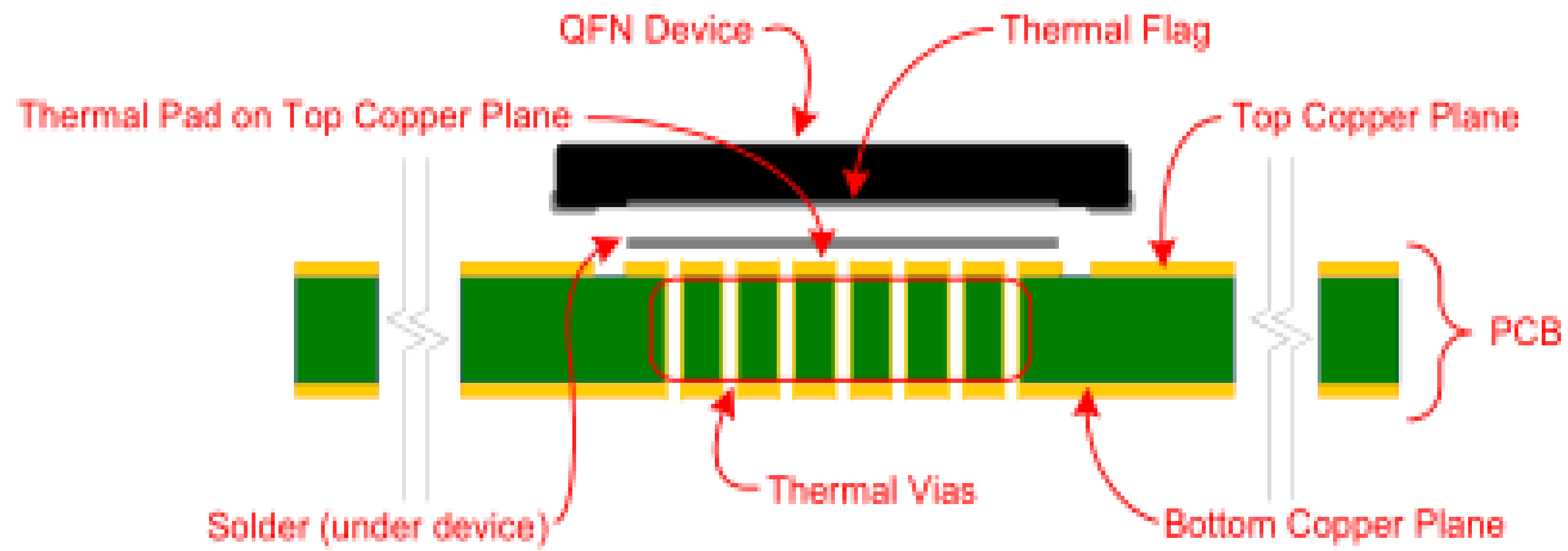
Calentamiento de las pistas



Disipación térmica



Disipación térmica



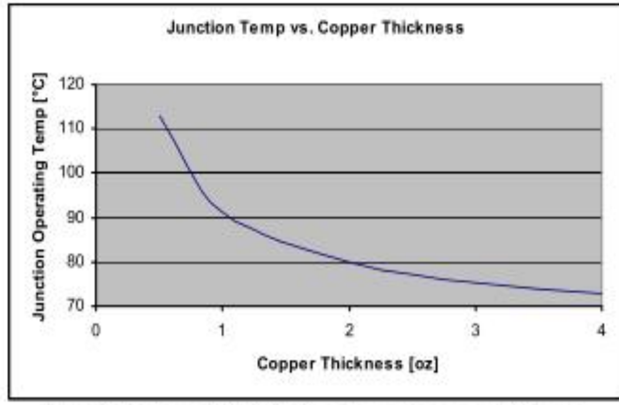


Figure 15a: Law of diminishing returns for copper thickness

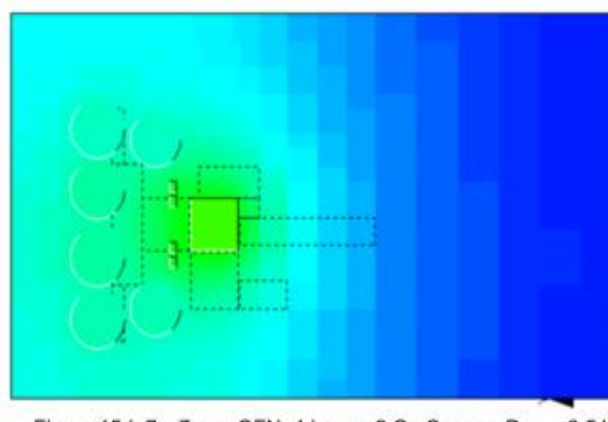


Figure 15d: 7 x 7 mm QFN, 4 Layer, 2 Oz Copper, P_{diss} = 3.5 W

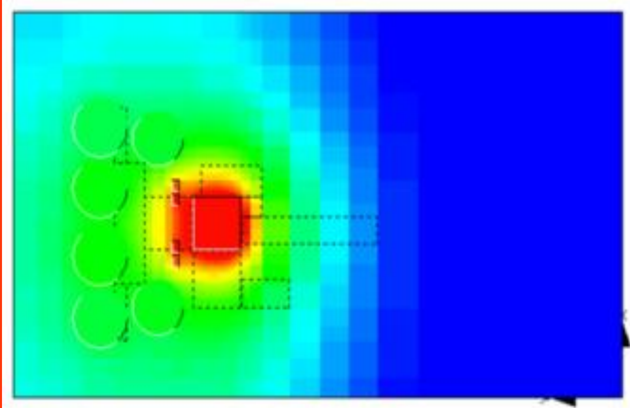


Figure 15b: 7 x 7 mm QFN, 4 Layer, ½ Oz Copper, P_{diss} = 3.5 W

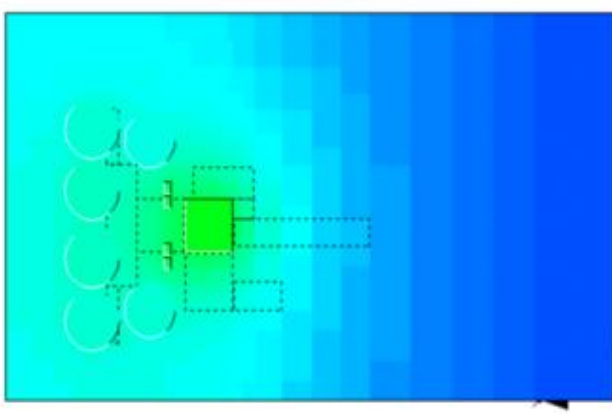
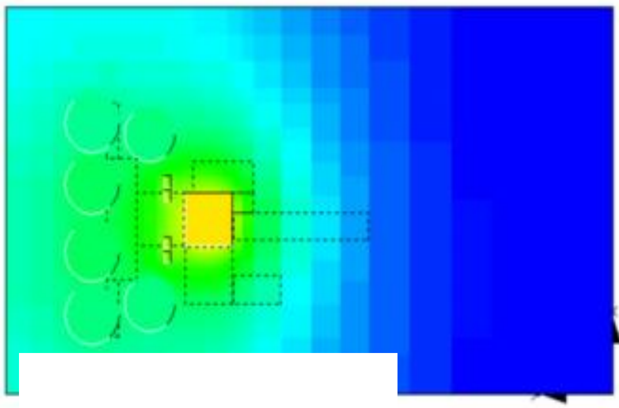


Figure 15e: 7 x 7 mm QFN, 4 Layer, 3 Oz Copper, P_{diss} = 3.5 W


z Copper, P_{diss} = 3.5 W

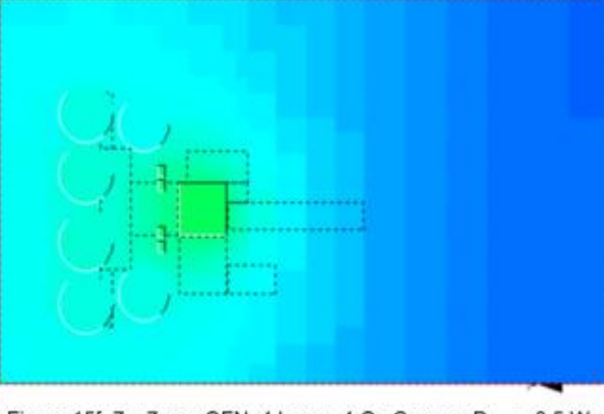
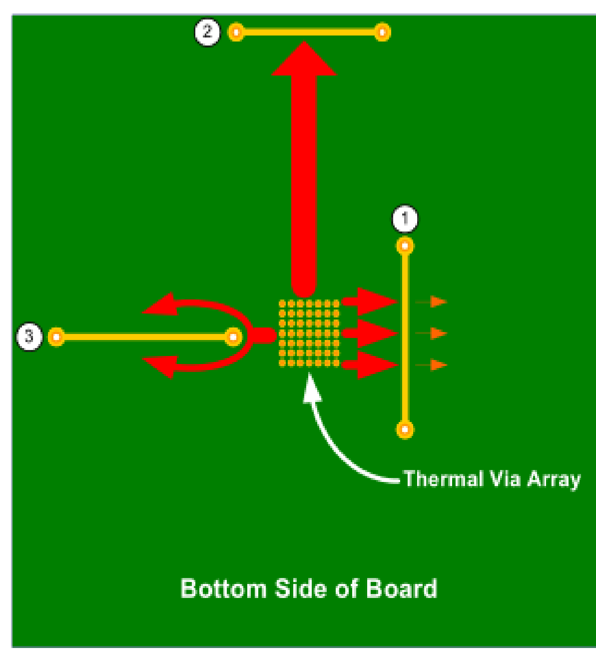
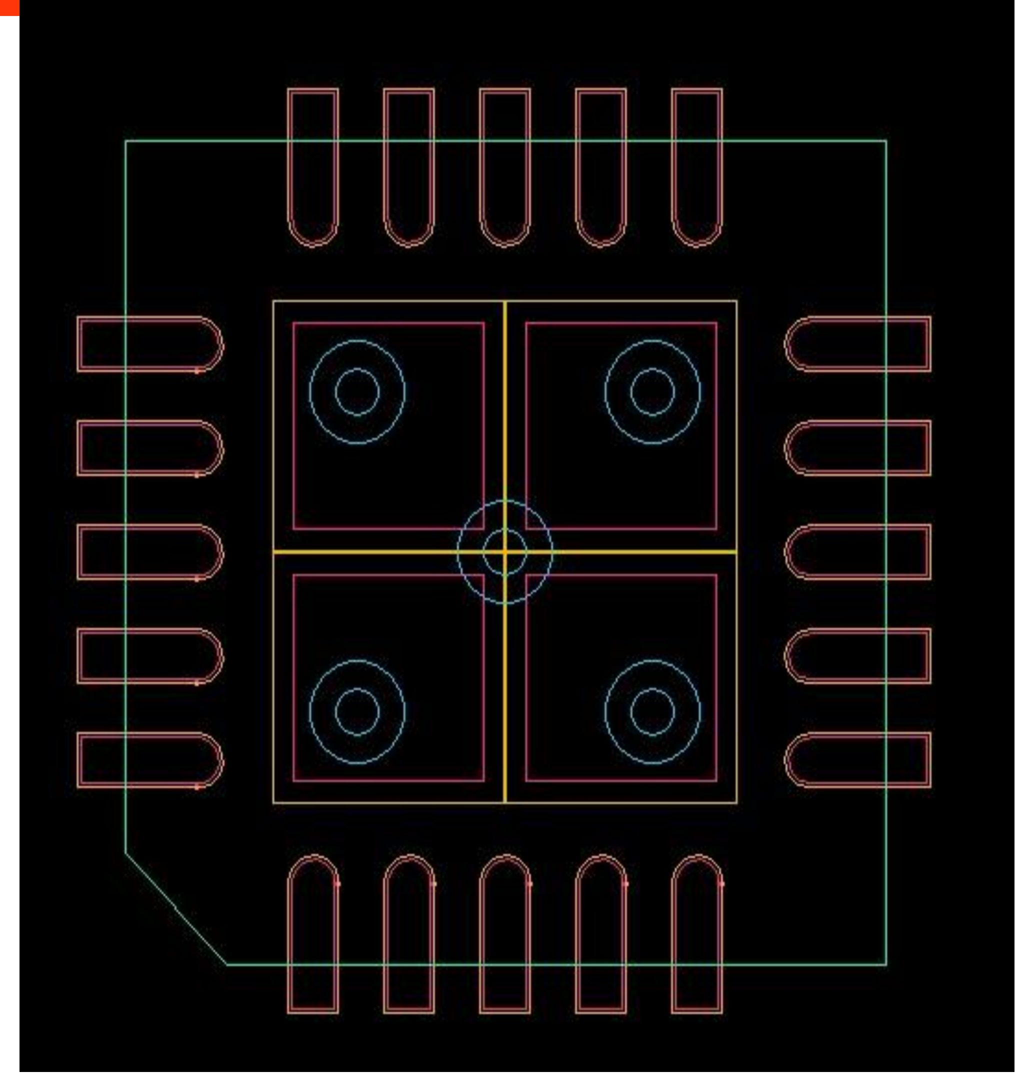


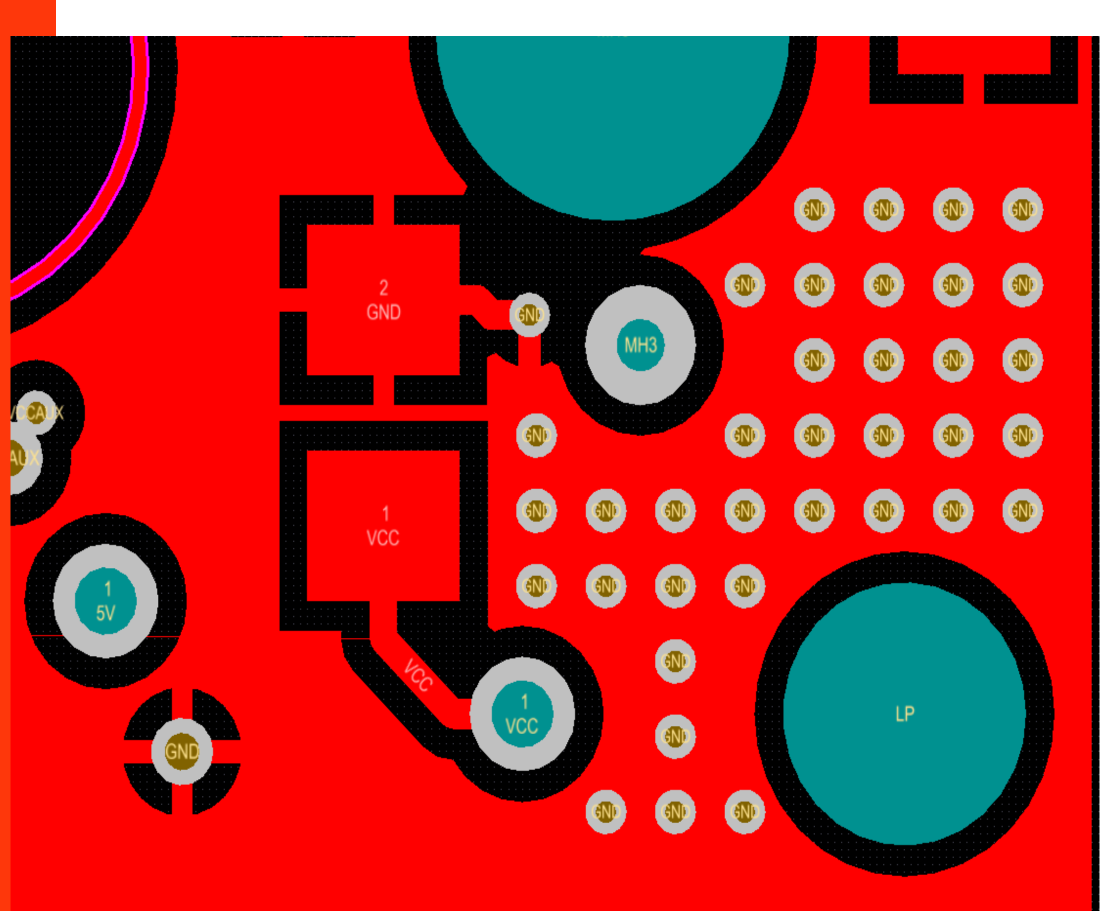
Figure 15f: 7 x 7 mm QFN, 4 Layer, 4 Oz Copper, P_{diss} = 3.5 W



Thermal Pads



Via Stiching:



PROCEDIMIENTO

http://wiki.altium.com/display/ADOH/Via+Stitching

Via Stiching:

Add Stitching to Net

Stitching Parameters

Net N1

Grid 1mm

Stagger alternate rows

Same Net Clearances

Applicable Rule (Via Stitching Constraint) detected. Default below will only be used as necessary.

Edit clearance rule...

Default Via/Pad Clearance 0.2mm

Min Boundary Clearance 0mm

Via Style

Diameters

Simple · Top-Middle-Bottom · Full Stack

Hole Size 0.3mm

Diameter 0.6mm

Load values from Routing Via Style Rule

Properties

Start Layer Top Layer

End Layer Bottom Layer

Solder Mask Expansions

Expansion value from rules

Specify expansion value 0.102mm

Force complete tenting on top

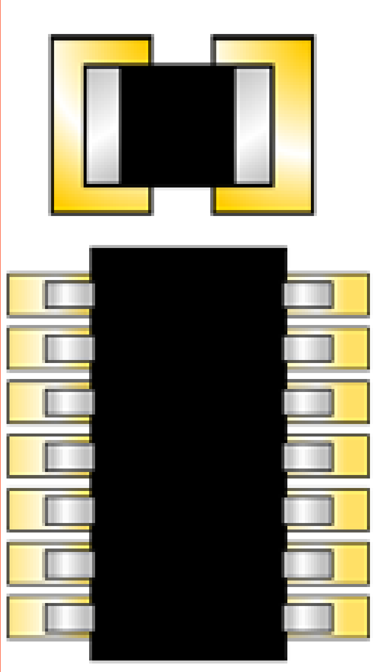
Force complete tenting on bottom

More Information...

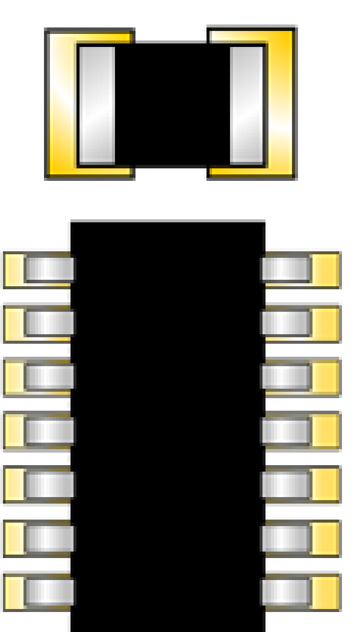
OK · Cancel

ugr Universidad de Granada
Departamento de Electrónica y Tecnología de Computadores

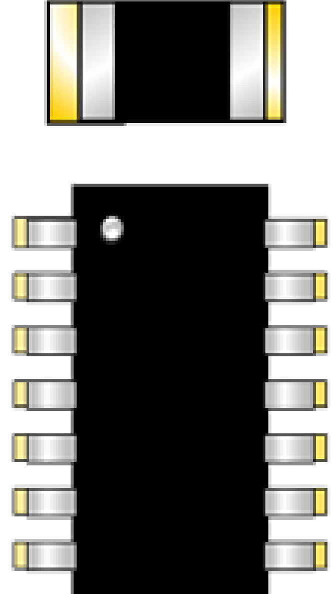
Pads for Density Levels



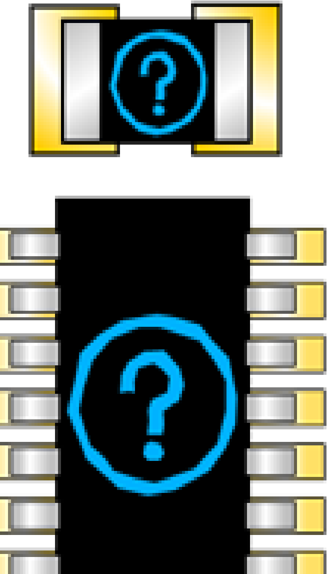
Density Level A
Very Robust
Solder Joint



Density Level B
General Purpose
Solder Joint



Density Level C
Minimal Solder Joint
High Density



CUSTOM
Mfr Recommended, or
User/Customer Required

Electrical Clearance

IPC 2221A: AC and pulsed voltages > 200V must consider dielectric and capacitive effects of substrate in addition to spacing.

Withstand Voltage	Min. Spacing
0-30 V	3.9 mil
31-150	24.0 mil
151-300	49.2 mil
301-500	98.4 mil

Selected References

IPC –2221A: "Generic Standard on PCB Design"
UL 8402: "Insulation Coordination Including Clearance and CreepageDistances for Electrical Equipment"
ANSI/ISA S82.01: "Safety Standard for Electrical and Electronic Test, Measuring, Controlling, and Related Equipment –General Requirements"
IEC 61010-1: "Safety Standard for Electrical and Electronic Test, Measuring, Controlling, and Related Equipment –Part 1: General Requirements"
UL 746E: "Standard Polymeric Material used in Printed Wiring Boards"
Web Site: http://www.energy.ece.uiuc.edu/balog