ACADEMIC COURSE 2023/2024

Controller for tuning a resonant cavity of a particle accelerator using a motorized plunger

AUTHOR:

Juan Alberto Serrano Redondo

SUPERVISED BY:

Sr. Andrés Roldán Aranda

DEPARTMENT:

Electronics and Computer Technology

UNIVERSIDAD DE GRANADA

Project title: plunger_07.PrjPcb			
Date: 22/10/2024	Revision: 0.7	Sheet 1 of 17	

Introduction

Objetives

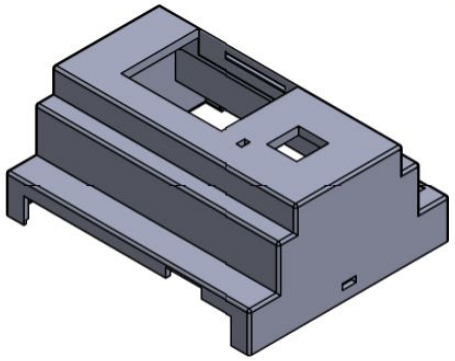
The aim of this project is to develop a motorized plunger control system using the ESP32 microcontroller for precise tuning of resonant cavities within a neutron accelerator. Resonant cavities play a crucial role in particle accelerators by maintaining electromagnetic fields that accelerate particles to high energies. The correct tuning of these cavities is essential for optimizing the accelerator's performance and ensuring minimal energy losses.

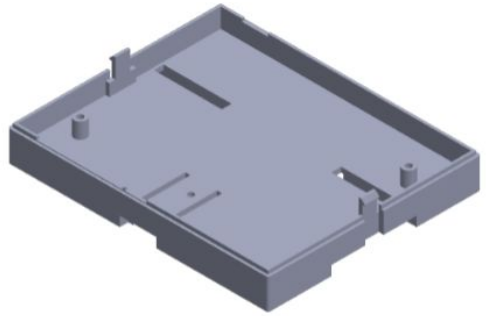
This device will control the positioning of critical components, such as plungers, within the cavities, ensuring that the accelerator operates at its optimal frequency. The motorized system allows for real-time adjustments, contributing to improved stability and performance.

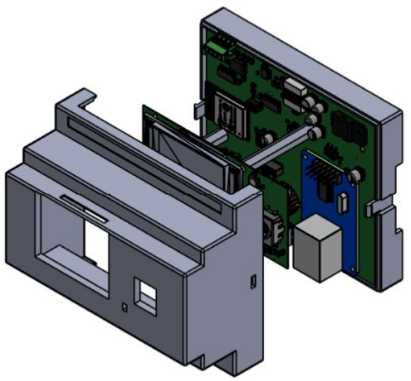
Motivation

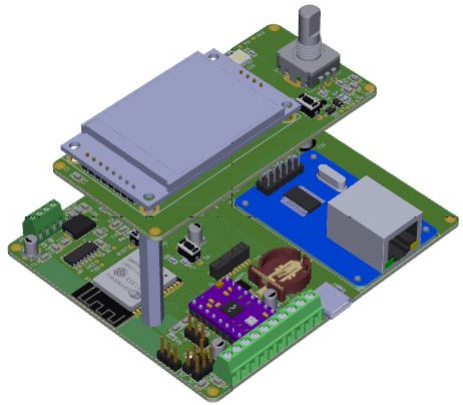
Advancements in particle accelerator technology not only drive scientific progress but also have direct applications in fields like medicine and industry. Precisely adjusting the components of these systems is essential for them to operate efficiently, and this project aims to address just that: developing a control system that allows for quick and accurate real-time adjustments.

The use of the ESP32 board as the brain of the control system opens up new possibilities for creating a modern, flexible, and adaptable solution. Through this project, we seek to simplify and automate processes that have traditionally been complex and time-consuming. This will not only improve the performance of accelerators but also make the operators' jobs easier, allowing them to focus on what truly matters: making discoveries that have the potential to change the world.









Resonant Cavity Motorized Tuning Controller

Device capable of controlling a motorized plunger to tune the resonant cavity of a particle accelerator

Designer's signature

Supervisor's signature

Sheet title: Introduction		
Project title: plunger_07.PrjPcb		
Desginer: Juan Alberto Serrano Redondo		
Date: 22/10/2024	Revision: 0.7	Sheet 2 of 17

Supervisor:
Sr. Andrés Roldán Aranda
Dpto. Electrónica y Tecnología de Computadores
University of Granada
C/ Fuente Nueva, s/n, 18001
Granada, Granada, Spain

Index

SECTION SHEET

Changelog

Revision 0.7

NEW

- Added draftsman documentation.

FIXED

- Ajusted PCBs desing.
- Ajusted the LCD height due to collisions in the user interface PCB.

Revision 0.6

NEW

- Added a multiboard project.
- Updated block diagram.

FIXED

- Ajusted the power budget.
- Readded the driver module due to soldering problems.

Revision 0.5

NEW

- Added a PCB template.
- Added spacers for the physical separation between the PCBs.
- Added the ribbon wire headers for the connection of the PCBs.
- Changed the motor driver module for the separated components to save space.

FIXED

- Swapped the RS232 for a RS3232.
- Relocated components in the PCB layout.
- Ajusted PCB tracks width.
- Improved routing.

Revision 0.4

NEW

- Added parameters for fabrication groups and fabrication order
- Added a typhical and maximum power budget.
- Given more info about ESP32 pins.
- Added a precise block diagram.
- Added tables with information for each component.
- Added a cover.

FIXED

- Reajust the PCB restricted area due to the antenna MCU specifications.
- Changed the USB-C footprint.
- Improved routing.
- Avoided disrupting the ESP32's strapping pins default configuration during boot.
- Swapped the DC/DC converters for avaliable models.

Revision 0.3

NEW

- Added PCB restricted area in the MCU antenna area.
- Added via stiching around all the PCBs.
- Improved routing.
- Avoided disrupting the ESP32's strapping pins default configuration during boot.
- Adopted JLCPCB design rules.

FIXED

- Changed numerical test point designators to net/rail names, to be quickly identified.
- Changed LCD, resistors and capacitors footprints.
- Corrected a faulty connection on the RS232.
- Adjusted voltage levels to ensure the correct functionality of the components according to the logic levels of the MCU.

Revision 0.2 [FIRST PCB]

NEW

- Schematic hierarchy and block diagram.
- Initial PCB layout
- Added a rotary encoder.
- Added a RGB led.
- Added footprints for all neccessary components to the PCB Library.
- Added explanatory footprints and photos to schematic ICs.
- Added board mounting holes (making use of the TFT LCD module mounting hole positions)
- Added fiducials
- Added a power-up button
- Added a power rail (24V-12V-5V-3V3)

FIXED

- Removed errors ethernet module.
- Removed errors in the motor driver.
- Changed ESD USB Protection IC.
- Changed the USB mini B for an USB C.
- Revised all passive components values and sizes to match existing component disponibility.
- Corrected various pin definitions from the ESP32-WROOM-32D symbol

REVISION 0.1 [FIRST VERSION]

NEW

- TFT LCD / SD card connections.
- Added a motor driver .
- Auto programming circuit.
- Added a rotary encoder.
- Added a ethernet module.
- Added a MAXRS232.
- Added a RTC module.

FIXED

--

Index and changelog

Index of the project and changelog of each revision

Designer's signature

Supervisor's signature

Sheet title: Index and changelog

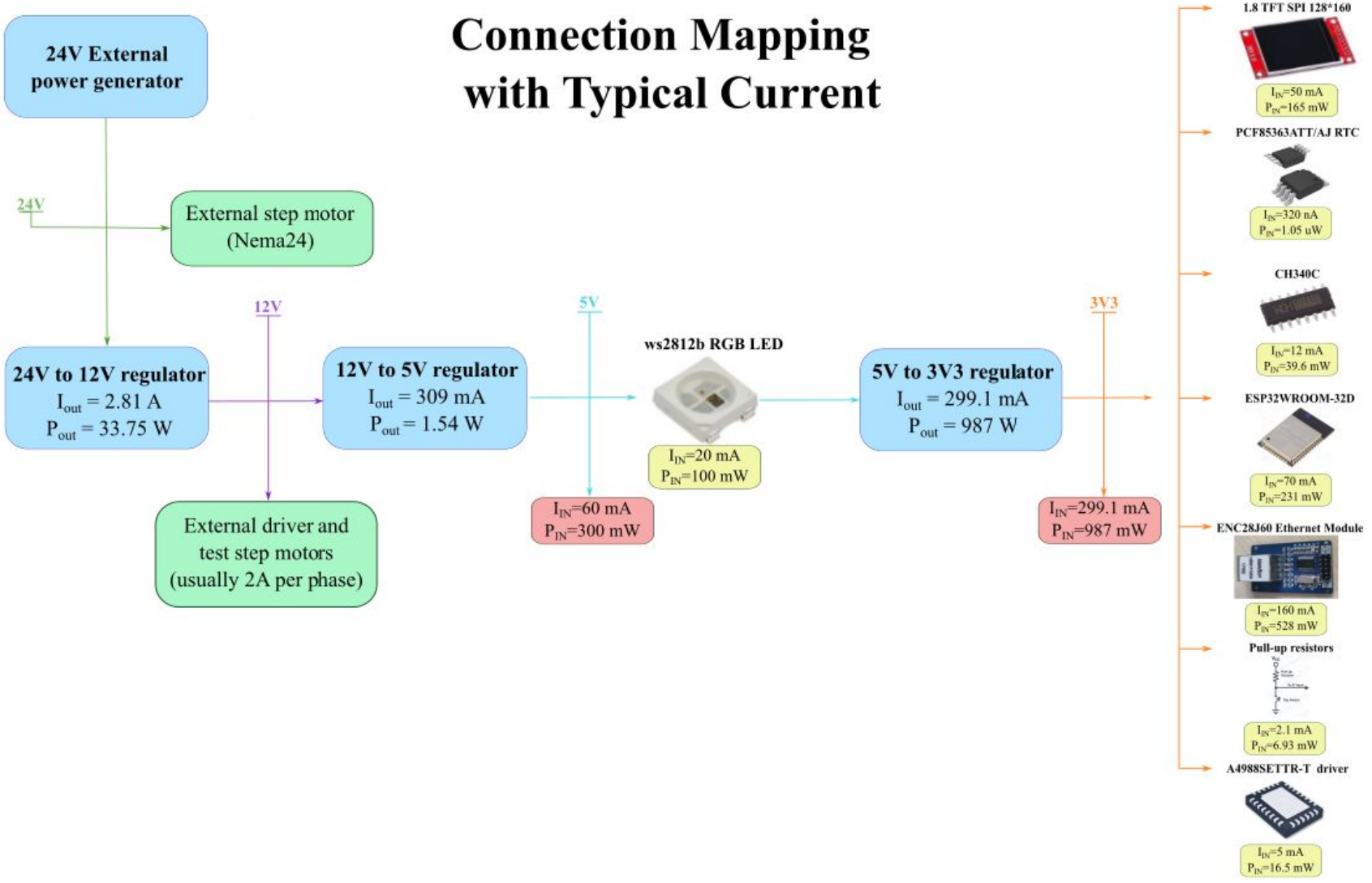
Project title: plunger_07.PrjPcb

Desginer: Juan Alberto Serrano Redondo

Date: 22/10/2024 | Revision: 0.7 | Sheet 3 of 17

Supervisor:
Sr. Andrés Roldán Aranda
Dpto. Electrónica y Tecnología de Computadores
University of Granada
C/ Fuente Nueva, s/n, 18001 Granada, Granada, Spain

Connection Mapping with Typical Current

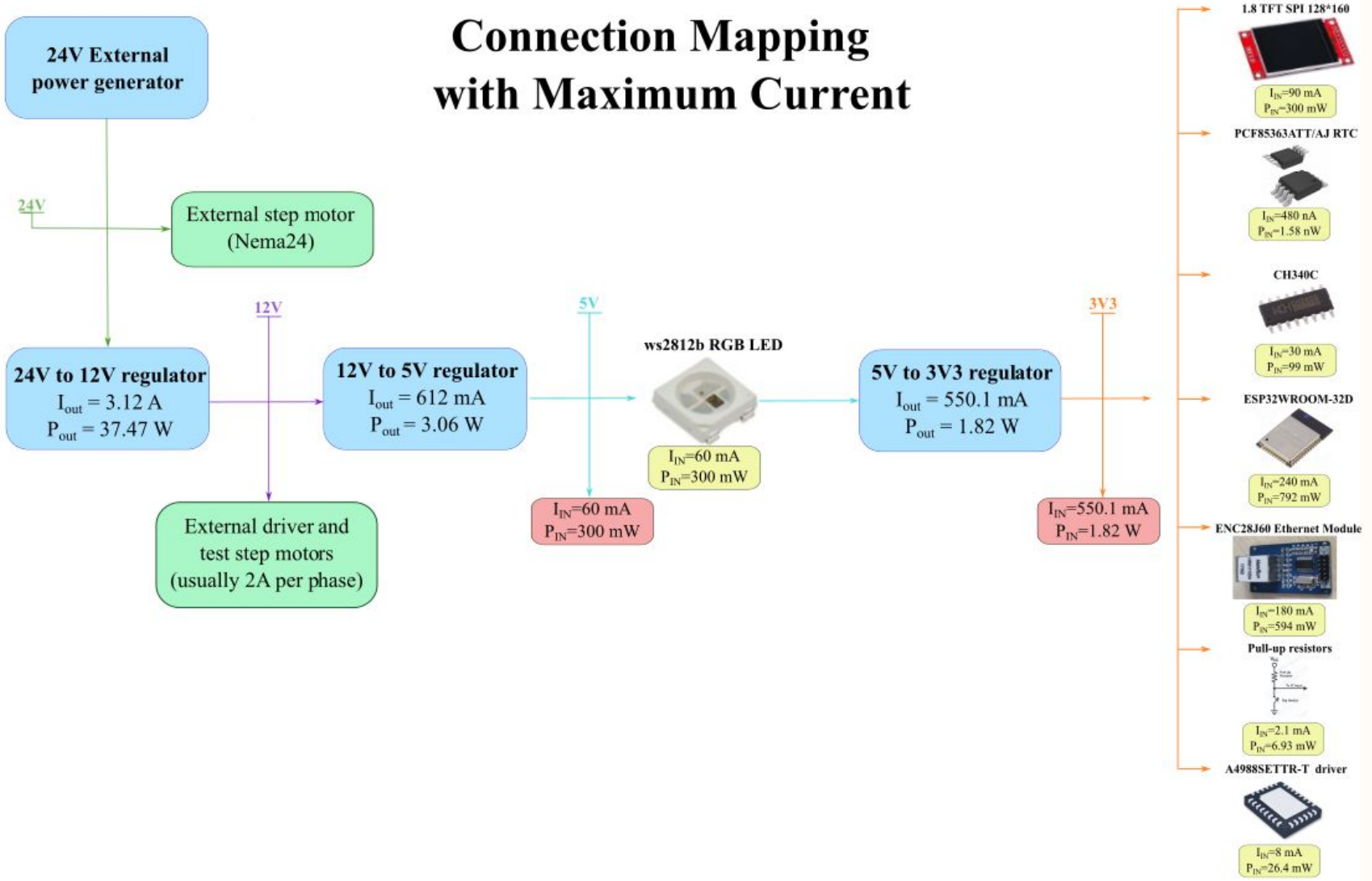


Typhical power budget

Connection mapping and power budget considering the typhical current consumption of the components.

Designer's signature	Sheet title: Typhical power budget		Supervisor: Sr. Andrés Roldán Aranda *Dpto. Electrónica y Tecnología de Computadores* *University of Granada* *C/ Fuente Nueva, s/n, 18001 Granada, Granada, Spain*
	Project title: plunger_07.PrjPcb		
Supervisor's signature	Desginer: Juan Alberto Serrano Redondo		
	Date: 22/10/2024	Revision: 0.7	Sheet 4 of 17

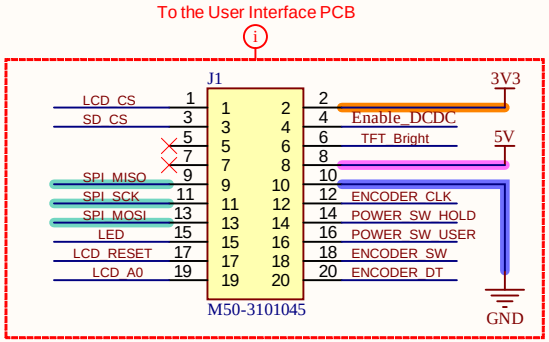
Connection Mapping with Maximum Current

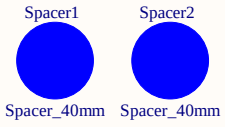


Maximum power budget

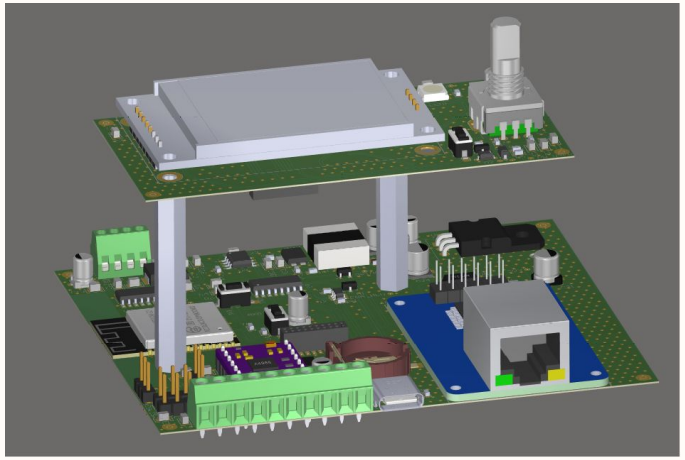
Connection mapping and power budget considering the maximum current consumption of the components.

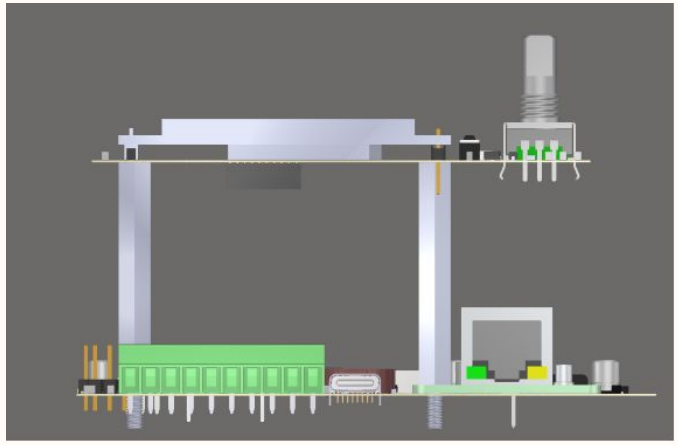
Designer's signature	Sheet title: Maximum power budget		Supervisor: Sr. Andrés Roldán Aranda *Dpto. Electrónica y Tecnología de Computadores* *University of Granada* *C/ Fuente Nueva, s/n, 18001* *Granada, Granada, Spain*
Supervisor's signature	Project title: plunger_07.PrjPcb		
	Desginer: Juan Alberto Serrano Redondo		
	Date: 22/10/2024	Revision: 0.7	Sheet 5 of 17





The connection between the two PCBs will be established using ribbon cables. Spacers are employed to maintain separation between the PCBs due to the structural design of the product enclosure.
Additionally, the ribbon cables are chosen for their flexibility and ability to manage multiple signal lines within a compact form, ensuring a reliable connection between the PCBs. The spacers provide the necessary physical separation to accommodate the box's designThis setup allows for easy assembly and maintenance of the electronic system within the product's housing.





Interconnection diagram

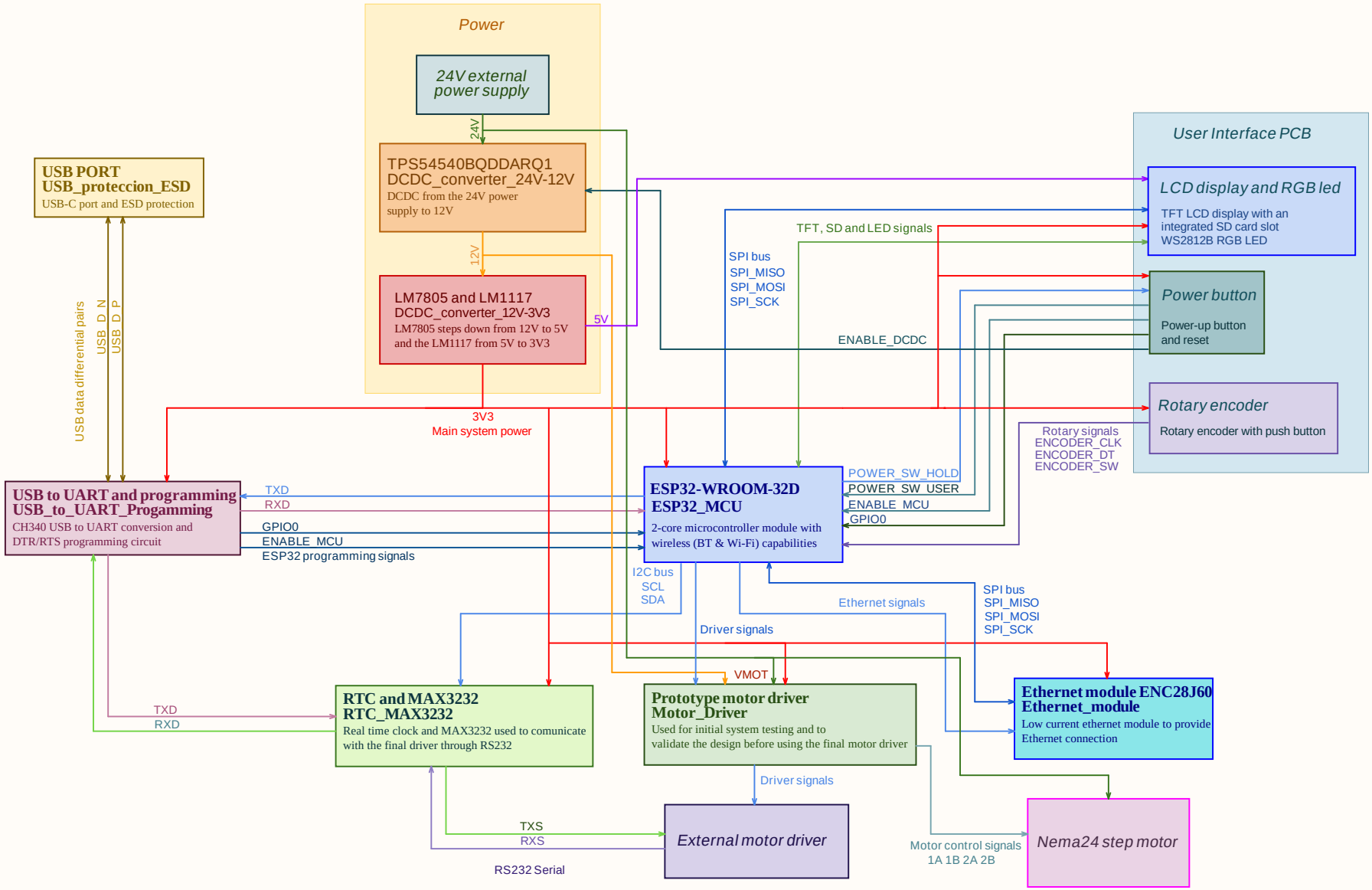
Connection diagram between the two designed PCBs

Designer's signature

Supervisor's signature

Sheet title: Interconnection diagram		
Project title: plunger_07.PrjPcb		
Desginer: Juan Alberto Serrano Redondo		
Date: 22/10/2024	Revision: 0.7	Sheet 6 of 17

Supervisor:
Sr. Andrés Roldán Aranda
Dpto. Electrónica y Tecnología de Computadores
University of Granada
C/ Fuente Nueva, s/n, 18001
Granada, Granada, Spain

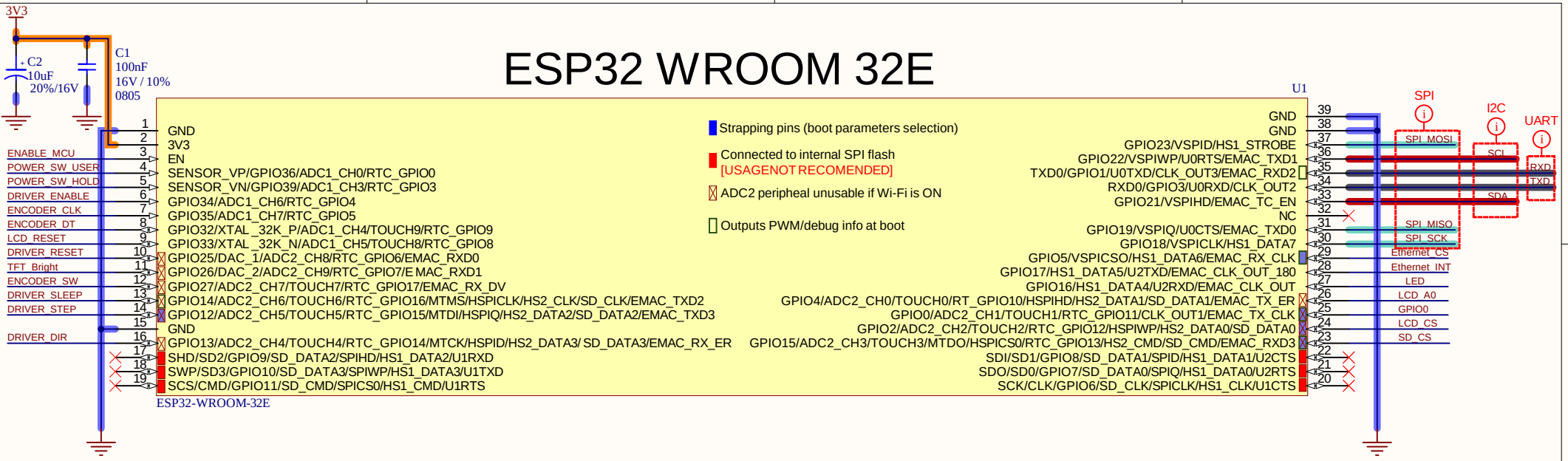


System blocks organization and connections

The project's global block diagram. Arrows show how modules are interconnected and include net names.

Designer's signature	Sheet title: System blocks organization and connections		Supervisor: Sr. Andrés Roldán Aranda *Dpto. Electrónica y Tecnología de Computadores* *University of Granada* *C/ Fuente Nueva, s/n, 18001* *Granada, Granada, Spain*
Supervisor's signature	Project title: plunger_07.PrjPcb		
	Desginer: Juan Alberto Serrano Redondo		
	Date: 22/10/2024	Revision: 0.7	Sheet 7 of 17

ESP32 WROOM 32E

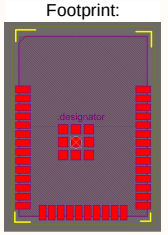


ESP-32-WROOM-32D	
CPU	Xtensa LX6 32 bits Dual core from 80 MHz to 240 MHz.
SRAM	520 kB (8kB SRAM in RTC)
FLASH	4 MB (larger avaliable)
ROM	448 kB
POWER SUPPLY	3.0 V to 3.6 V
CURRENT CONSUMPTION	Minimum current required to be delivered: 500 mA Average current consumption: 80 mA Sleep: 2.5 uA (10uA RTC+ RTC memory) Low consumption:>150 uA
TEMPERATURE RANGE	-40ºC to 85ºC
Wi-Fi	802.11 b/g/n (802.11n up to 150 Mbps)
Wi-Fi MODES	Station / SOFTAP / SOFTAP + STATION / P2P
NETWORK PROTOCOL	Ipv4 / ipv6 / SSL / TCP / UDP / HTTP / FTP / MQTT

ESP-32-WROOM-32D	
BLUETOOTH	Bluetooth v4.2 BR/EDR and Bluetooth LE specification.
HW ENCRYPTATION	Yes
GPIO	38
DAC	SAR 12 bits 12 Channels.
INTERFACES	UART/SDIO/SPI/I2C/I2S/IR REMOTE CONTROL GPIO/ADC/DAC/TOUCH/PWM/LED/SD card
TOUCH SENSOR	Yes (8 Channels)
TEMPERATURE SENSOR	Yes
HALL EFECT SENSOR	Yes
DIMMENSIONS	18 × 25.5 × 3.1 mm^3
PRICE	2.85 € https://www.lcsc.com/

Real model:

Footprint:



Fiducial markers are used by AOI machines to accurately locate and orient the PCB. By recognizing fiducials, the machine can align the PCB accurately and place components precisely where they need to be.

The absolute maximum current drawn per GPIO is 40 mA.

ESP32-WROOM-32E MCU

This module integrates an ESP32-D0WD chip, a 240 MHz, dual-core processor with Wi-Fi and Bluetooth capabilities. This sheet describes its hardware configuration and I/O pins

Designer's signature

Supervisor's signature

Sheet title: ESP32-WROOM-32E MCU

Project title: plunger_07.PrjPcb

Desginer: Juan Alberto Serrano Redondo

Date: 22/10/2024 | Revision: 0.7 | Sheet 8 of 17

Supervisor:
Sr. Andrés Roldán Aranda
Dpto. Electrónica y Tecnología de Computadores
University of Granada
C/ Fuente Nueva, s/n, 18001 Granada, Granada, Spain

USB and ESD protection

'SH' pads are the USB connector metal shield, which is structural. This particular connector has 4 which are connected to GND following the datasheet recomendations.

USB-C is USB 2.0 capable, fairly high speed, and althought we may not use all of its capabilities, its data traces need special attention as they are

Ferrite Bead as EMI supressor. Works similar to an inductor: high impedance for high frequencies and very low for DC

- 2 data lines protection
- Protects V_{BUS}
- Very low capacitance: 3.5 pF max.
- Very low leakage current: 150 nA max.
- SOT-666 and SOT23-6L packages
- RoHS compliant

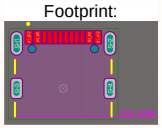
An USB-C has been chosen mainly because of the European Parliament and Council Directive 2022/2380 mandates USB-C ports for all new electronical devices sold in the European Union starting December 28, 2024. This aligns with the increasing adoption of USB-C across electronic devices.

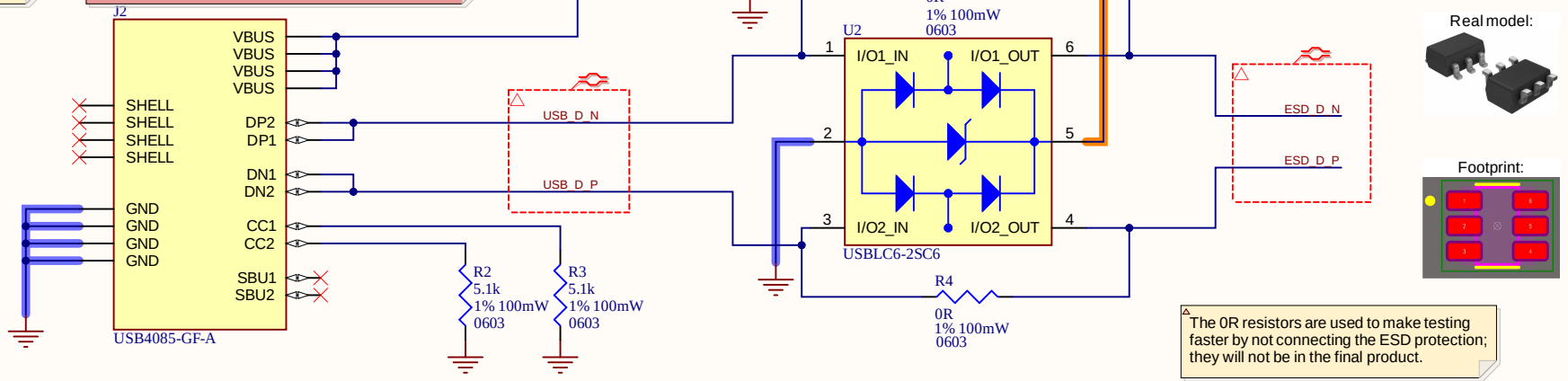
Pulling down both CC1 and CC2 pins to ground with two 5% 5.1K resistors tells the USB host that you want to draw up to 1.5 A@5 V or 3.0 A@5 V for powering your device.Special attention as they are differential. https://pcbartists.com/design/embedded/how-to-replace-microusb-with-usb-c-connector/

ESD protection IC should be as close as possible to the USB connector to avoid damaging any other circuits.

Real model:

Footprint:





Real model:

Footprint:

The 0R resistors are used to make testing faster by not connecting the ESD protection; they will not be in the final product.

USB4105-GF-A (USB-C)	
VOLTAGE RATING	48 V DC.
CURRENT RATING	5 A collectively for V_{BUS} pins 6.25 A collectively for GND pins 1.25 A collectively for A5/B5 pins 0.25 A per pin for all other pins
OPERATING TEMPERATURE	-40ºC to 85ºC
USB DEVICE INTERFACE	2.0
TERMINATION	Surface Mount
DIMENSION	8.64 × 7.35 × 2.56 mm^3
PRICE	0.93 € https://www.mouser.es/

USBLC6-2SC6	
VOLTAGE CLAMP	17 V
BREAKDOWN VOLTAGE BETWEEN V_{BUS} AND GND	6 V
MAX LEAKAGE CURRENT	150 nA
USB DEVICE INTERFACE	2.0
FORWARD VOLTAGE	1.1 V
DIMENSION	1.45 × 1.75 × 3.05 mm^3
PRICE	0.33 € https://www.mouser.es/

USB connector and ESD protection circuit

USB is used as a programming interface. Since it's an external connector, it needs to have a protection circuit against electro-static discharge (ESD) and noise.

Designer's signature

Supervisor's signature

Sheet title: USB connector and ESD protection circuit

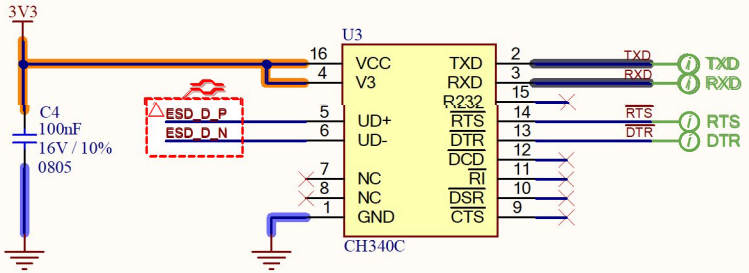
Project title: plunger_07.PrjPcb

Desginer: Juan Alberto Serrano Redondo

Date: 22/10/2024 | Revision: 0.7 | Sheet 9 of 17

Supervisor:
Sr. Andrés Roldán Aranda
Dpto. Electrónica y Tecnología de Computadores
University of Granada
C/ Fuente Nueva, s/n, 18001
Granada, Granada, Spain

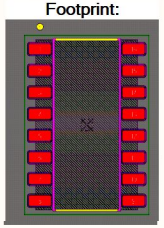
USB to UART

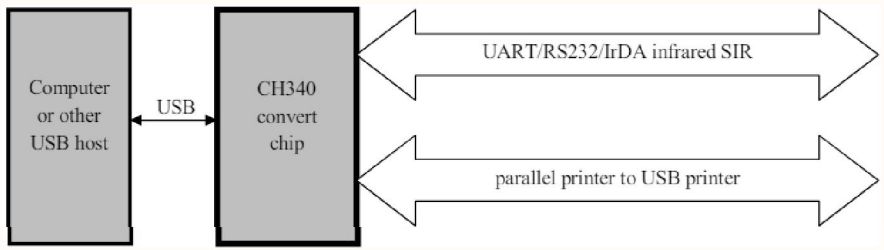


CH340C	
SUPPLY VOLTAGE	3.0 V to 3.3 V
SUPPLY CURRENT	30 mA (max) 12 mA (typ)
AMBIENT TEMPERATURE	-20℃ to 70℃
COMMUNICATION BAUD RATE	50 bps to 2Mbps
USB DEVICE INTERFACE	2.0
DIMENSION	3.9 × 1.27 mm³
PRICE	0.68 € https://www.mouser.es/

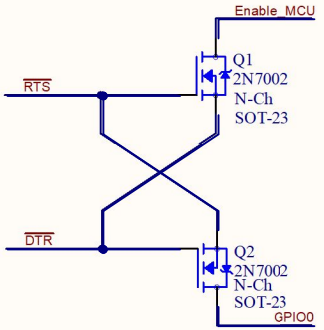
Real model:

Footprint:





Programming Circuit



ESP32 GPIO0 is a Strapping pin. Strapping pins modify the device's boot mode during chip reset. GPIO0 is pulled up during reset by default. ENABLE_MCU is pulled up by an external pullup resistor

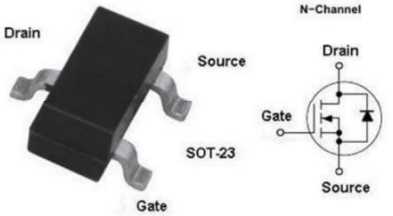
When GPIO0 is HIGH, it boots from internal SPI memory, but when it's LOW the boot sequence changes to 'Download' and we can upload a program to the MCU.

[v06 VALIDATION NOTE]

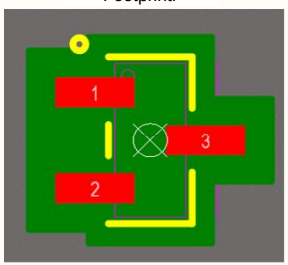
This circuit works correcly, the programming signaling sequence (RESET to Low, then GPIO0 to low) is correct and we can program the MCU.

DTR	RTS	ENABLE_MCU	GPIO0
0	0	1	1
0	1	1	0
1	0	0	1
1	1	1	1

Real model:



Footprint:



USB to UART and MAX232

This circuit allows a computer to the ESP32 via USB so it can be reprogrammed. MAX232 is used to comunicate with the motor driver by converting voltage levels between an RS-232 serial port and TTL.

Designer's signature

Supervisor's signature

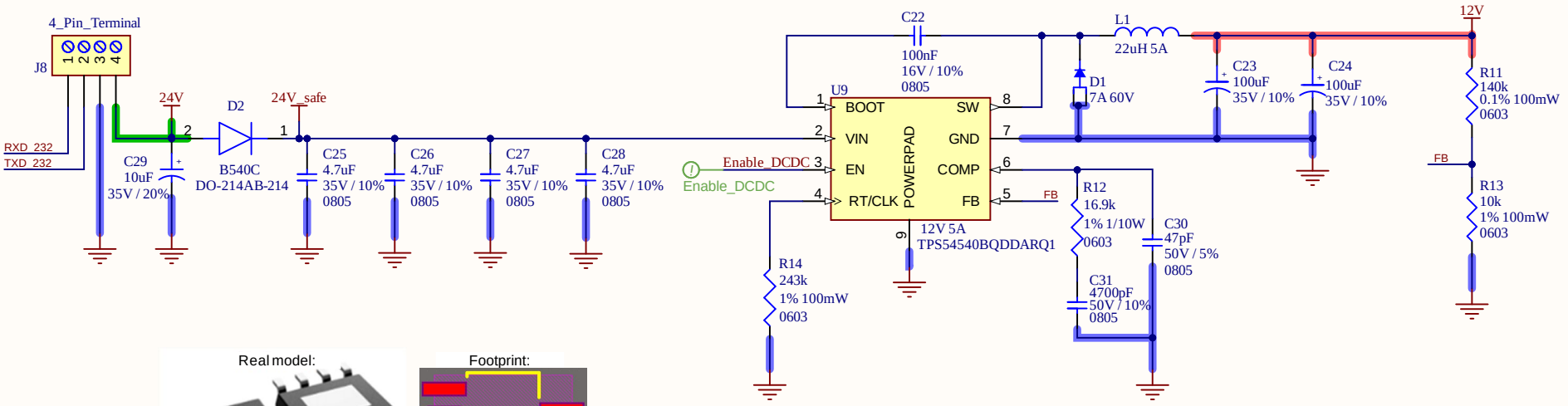
Sheet title: USB to UART and MAX232

Project title: plunger_07.PrjPcb

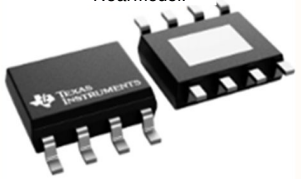
Desginer: Juan Alberto Serrano Redondo

Date: 22/10/2024 | Revision: 0.7 | Sheet 10 of 17

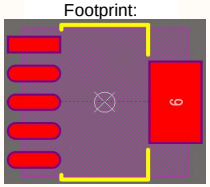
Supervisor:
Sr. Andrés Roldán Aranda
Dpto. Electrónica y Tecnología de Computadores
University of Granada
C/ Fuente Nueva, s/n, 18001 Granada, Granada, Spain



Real model:



Footprint:



PIN		I/O	DESCRIPTION
NAME	NO.		
BOOT	1	I	A bootstrap capacitor is required between BOOT and SW. If the voltage on this capacitor is below the minimum required to operate the high side MOSFET, the MOSFET stops switching until the capacitor is refreshed.
COMP	6	I	Error amplifier output and input to the output switch current (PWM) comparator. Connect frequency compensation components to this pin.
EN	3	I	Enable pin, with internal pullup current source. Pull below 1.2 V to disable. Float to enable. Adjust the input undervoltage lockout with two resistors. See the *Enable and Adjusting Undervoltage Lockout* section.
FB	5	I	Inverting input of the transconductance (gm) error amplifier.
GND	7	—	Ground
RT/CLK	4	I	Resistor Timing and External Clock. An internal amplifier holds this pin at a fixed voltage when using an external resistor to ground to set the switching frequency. If the pin is pulled above the PLL upper threshold, a mode change occurs and the pin becomes a synchronization input. The internal amplifier is disabled and the pin is a high impedance clock input to the internal PLL. If clocking edges stop, the internal amplifier is reenabled and the operating mode returns to resistor frequency programming.
SW	8	O	The source of the internal high-side power MOSFET and switching node of the converter.
VIN	2	I	Input supply voltage is connected to this pin with a 4.5-V to 42-V operating range.
PowerPAD	9	—	GND pin must be electrically connected to the exposed pad on the printed-circuit-board for proper operation.

TPS54540B-Q1	
INPUT VOLTAGE	4.5 V to 42 V
OUTPUT VOLTAGE	0.8 V to 58.8 V
CURRENT	Quiescent Current: 146 uA Shutdown Current: 2 uA
OUTPUT CURRENT	Up to 5 A
SWITCHING FREQUENCY	100-kHz to 2.5-MHz Adjustable
STORAGE TEMPERATURE	–40°C to 125°C
SYNCHRONOUS RECTIFIER	No
DIMENSION	4.89 mm × 3.90 mm
PRICE	4.95 € https://www.mouser.es/

DCDC converter 24V to 12V

TPS54540BQDDARQI dc-dc buck converter. The converter is designed to step down a 12V input voltage to a regulated 5V output voltage at up to 5A of current.

Designer's signature

Supervisor's signature

Sheet title: DCDC converter 24V to 12V

Project title: plunger_07.PrjPcb

Desginer: Juan Alberto Serrano Redondo

Date: 22/10/2024 | Revision: 0.7 | Sheet 11 of 17

Supervisor:
Sr. Andrés Roldán Aranda
Dpto. Electrónica y Tecnología de Computadores
University of Granada
C/ Fuente Nueva, s/n, 18001
Granada, Granada, Spain

LM7805
Suposing a Ta=30ºC
Pd=(12-5) V*0.66 A=4.62 W
RoJA=65ºC/W
Tj=30ºC+4.62W*65ºC/W=330.3ºC
Tj=[0,125]ºC
We need disipator.

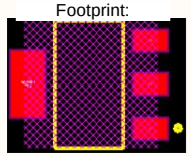
With a heatsink with a thermal resistance of 9ºC/W.

LM7805 RoJC=5ºC/W
RoCS=2ºC/W
RoSA=9ºC/W
RoJA=16ºC/W

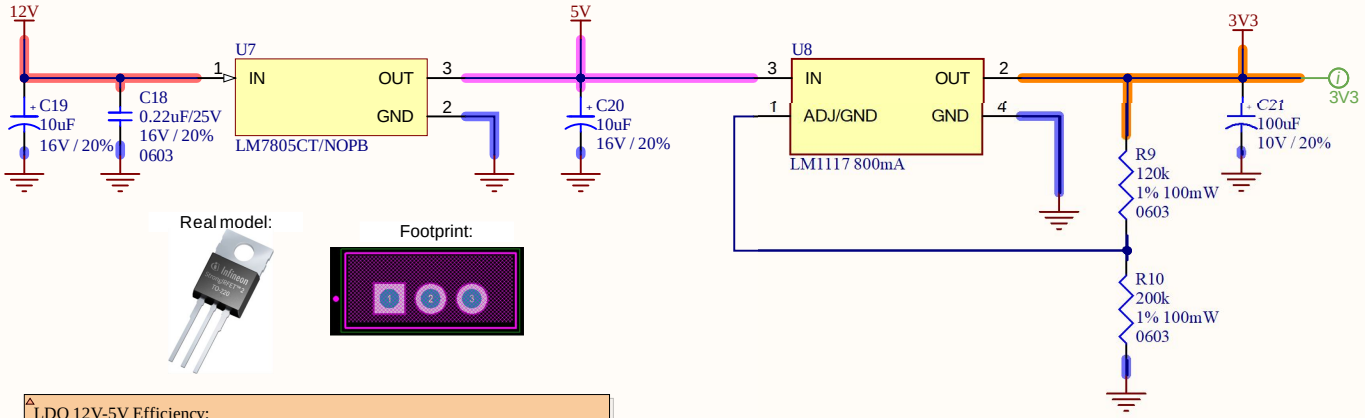
Tj=30ºC+4.62W*16ºC/W=103.92ºC

Real model:

Footprint:



LM1117
Suposing a Ta=30ºC
Pd=(5-3.3) V*0.7 A=1.19 W
RoJA=61.6ºC/W
Tj=30ºC+1.19W*61.6ºC/W=103.304ºC
Tj=[0,125]ºC



Real model:

Footprint:

LDO 12V-5V Efficiency:
Efficiency (ef) = (5 V / 12 V) x (Iout / (Iout + IGND)) x 100% = 41%
We need 3.06 W at the 5 V power rail. Considering the LDO efficiency of 41%, the required power at the LDO input is 3.06 W / 0.41 = 7.47W.
Therefore, the current needed from the 12 V power rail is 7.47 W / 12 V = 0.623 A, plus the consumption of the 12 V power rail devices.

LDO 5V-3.3V Efficiency:
Efficiency (ef) = (3.3 V / 5 V) x (Iout / (Iout + IGND)) x 100% = 66%
We need 1.82 W at the 3.3 V power rail. Considering the LDO efficiency of 66%, the required power at the LDO input is 1.82 W / 0.66 = 2.76 W.
Therefore, the current needed from the 5V power rail is 2.76 W / 5 V = 0.552 A. Adding the consumption of the 5 V power rail devices, which is 60 mA, the total current required is 0.552 A + 0.06 A = 0.612 A.

LM7805	
INPUT VOLTAGE	7V to 25 V
OUTPUT VOLTAGE	5 V ± 1%
OUTPUT CURRENT	1.5 A
OPERATING TEMPERATURE	0°C to 125°C
DIMENSION	16 mm × 10.5 mm
PRICE	0.15 € https://www.lcsc.com/

LM1117	
INPUT VOLTAGE	4.75 V to 10 V
OUTPUT VOLTAGE	3.3 V ± 1%
OUTPUT CURRENT	800 mA
OPERATING TEMPERATURE	0°C to 125°C
DIMENSION	7.3 mm × 6.7 mm
PRICE	0.14 € https://www.lcsc.com/

12V to 3.3V power rail

These voltage regulators are designed to provide an output voltage from a 12V input voltage. The LM7805 steps down the 12V input voltage to 5V, while the LM1117 further reduces it to a regulated 3.3V output.

Designer's signature

Supervisor's signature

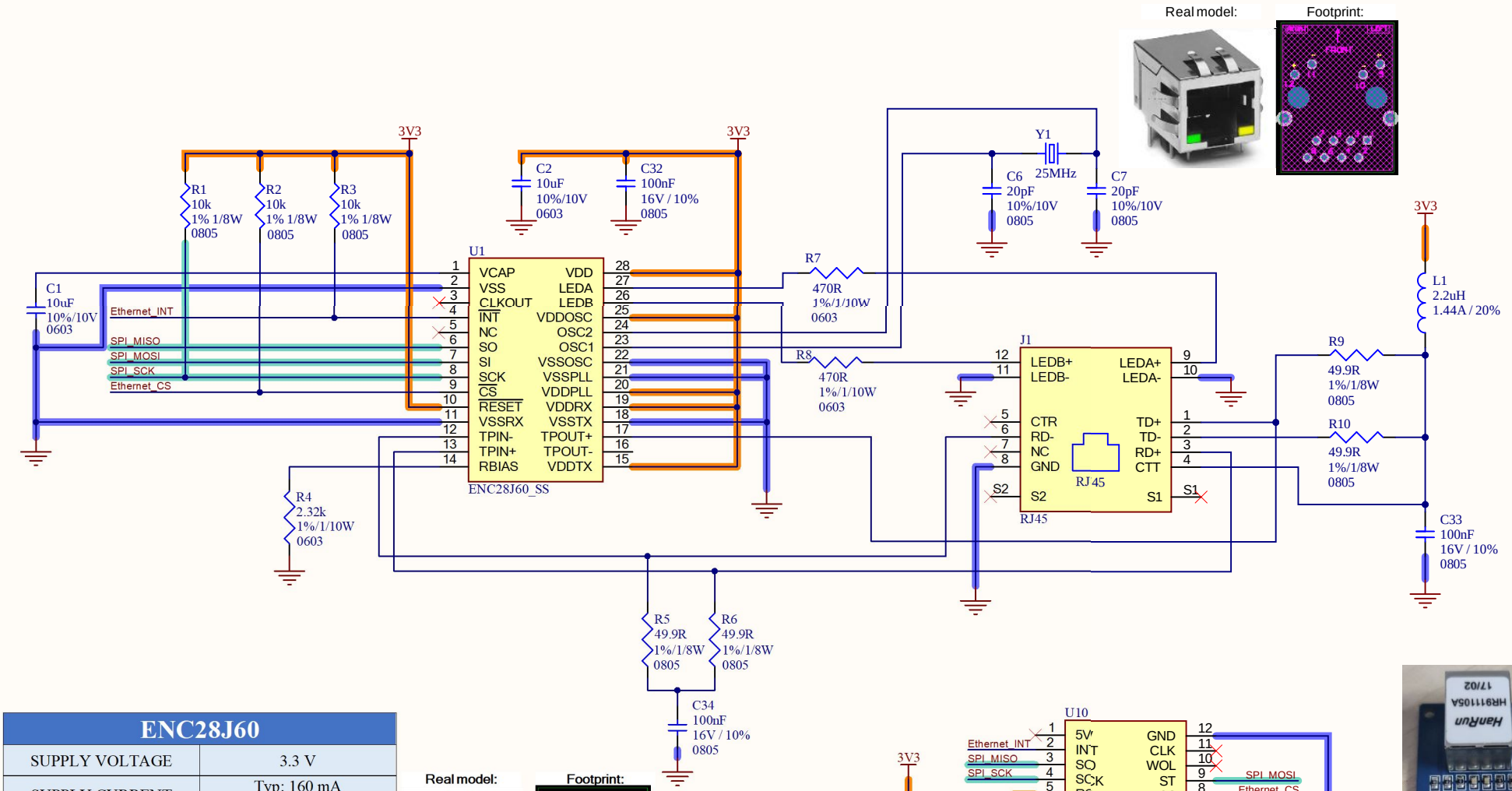
Sheet title: 12V to 3.3V power rail

Project title: plunger_07.PrjPcb

Desginer: Juan Alberto Serrano Redondo

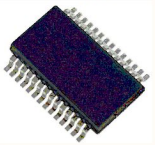
Date: 22/10/2024 | Revision: 0.7 | Sheet 12 of 17

Supervisor:
Sr. Andrés Roldán Aranda
Dpto. Electrónica y Tecnología de Computadores
University of Granada
C/ Fuente Nueva, s/n, 18001 Granada, Granada, Spain

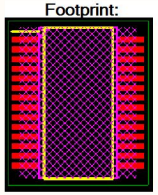


ENC28J60	
SUPPLY VOLTAGE	3.3 V
SUPPLY CURRENT	Typ: 160 mA Max: 180 mA
CLOCK IN FREQUENCY	25 MHz
OPERATING TEMPERATURE	-65°C to 150°C
PRICE	2.00 € https://es.aliexpress.com/

Real model:



Footprint:



ENC28J60 Module 12 pin version

The ENC28J60 is used to provide Ethernet connection to the product.
It has low current consumption and can be powered with either 5V or 3.3V.

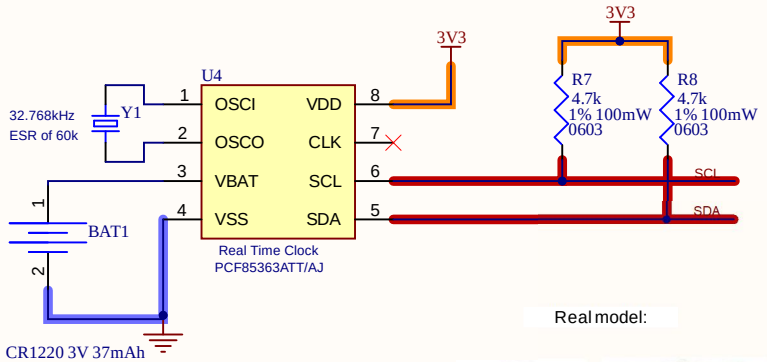
Designer's signature

Supervisor's signature

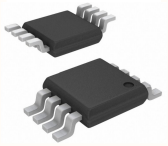
Sheet title: ENC28J60 Module		
Project title: plunger_07.PrjPcb		
Desginer: Juan Alberto Serrano Redondo		
Date: 22/10/2024	Revision: 0.7	Sheet 13 of 17

Supervisor:
Sr. Andrés Roldán Aranda
Dpto. Electrónica y Tecnología de Computadores
University of Granada
C/ Fuente Nueva, s/n, 18001
Granada, Granada, Spain

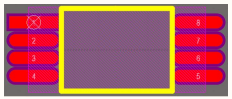
RTC PCF853663ATT/AJ



Real model:



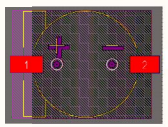
Footprint:

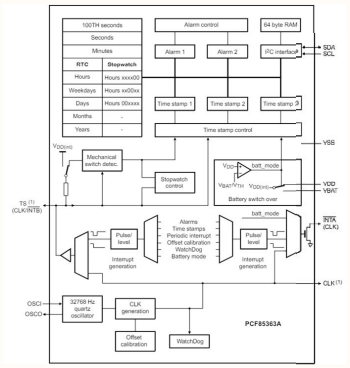


The RTC consumption when the main power system is not providing power is typically about 280 nA. With a CR1210 lithium cell battery that has a capacity of 37 mAh, the battery will last for:
37mAh / 280nA = 15.1 years

Real model:

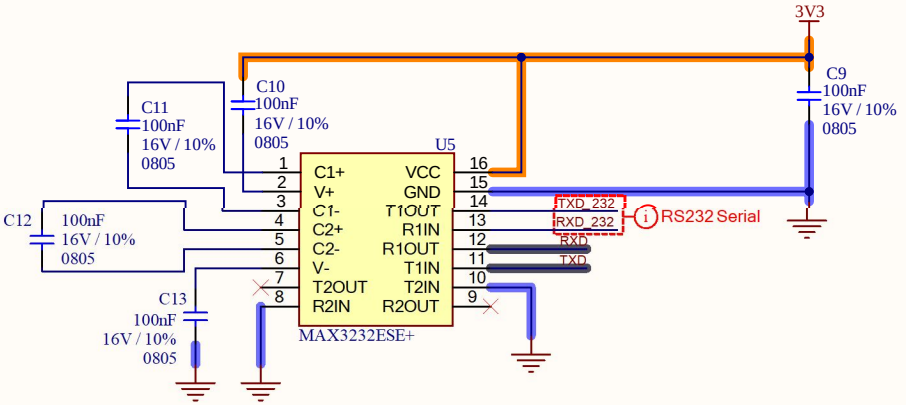
Footprint:



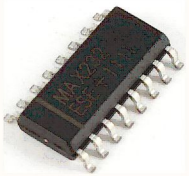


PCF85363ATT/AJ	
SUPPLY VOLTAGE	0.9 V to 5.5 V
SUPPLY CURRENT	Typ:320 nA Max: 480 nA @25ºC Typ:370 nA Max: 550 nA @50ºC Typ:590 nA Max: 885 nA @85ºC Typ: 10 uA I2C active
COMUNICATION INTERFACE	Two line I2C bus
OPERATING TEMPERATURE	-40ºC to 85ºC
DIMENSION	2.9 x 2.9 mm
PRICE	1.54 € https://www.lcsc.com/

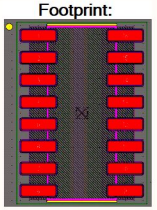
MAX3232



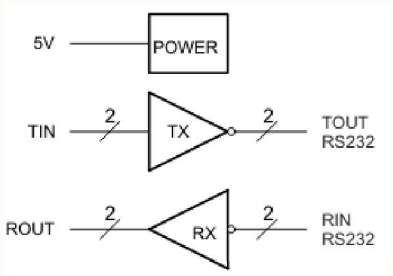
Real model:



Footprint:



The MAX3232 device is a dual driver/receiver that includes a capacitive voltage generator to supply TIA/EIA-232-F voltage levels from a single 3V3 supply.



MAX232	
SUPPLY VOLTAGE	3 V to 5.5 V
SUPPLY CURRENT	Typ: 0.3 mA (No load) Max: 1 mA (No load)
Driver Slew Rate	30 V/us
OPERATING TEMPERATURE	-40ºC to 85ºC
DIMENSION	9.9 x 6 mm
PRICE	2.39 € https://es.aliexpress.com/

RTC and RS3232

The RTC keeps track of the date, hour and day of the week even when the main power source is turned off.

Designer's signature

Supervisor's signature

Sheet title: RTC PCF85363ATT and RS3232

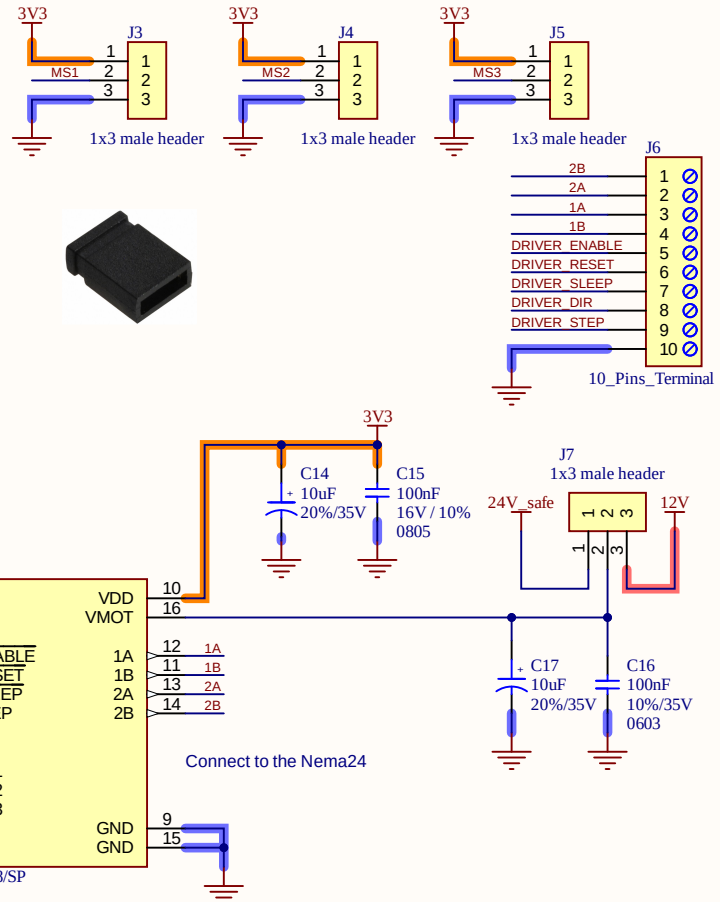
Project title: plunger_07.PrjPcb

Desginer: Juan Alberto Serrano Redondo

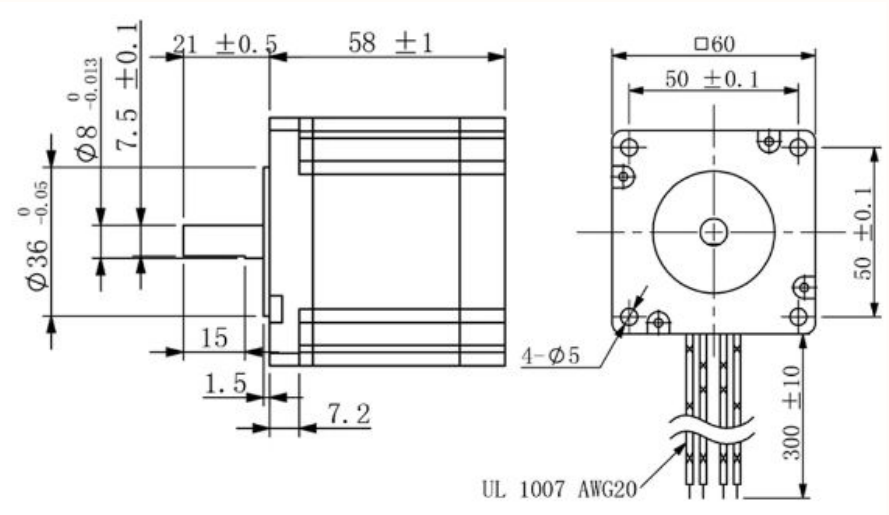
Date: 22/10/2024 | Revision: 0.7 | Sheet 14 of 17

Supervisor:
Sr. Andrés Roldán Aranda
Dpto. Electrónica y Tecnología de Computadores
University of Granada
C/ Fuente Nueva, s/n, 18001
Granada, Granada, Spain

Motor Driver



Nema24



Model	24CS22C-400
Phase Number	2
Step Angle (o)	1.8°±5%
Holding Torque (N.m)	2.2N.m
Rated Current (A)	4.0A
Phase Inductance (mH)	1.30mH±20%
Phase Resistance (ohm)	0.35ohm±10%
Number of Lead	4
Rotor Inertia (g.cm²)	490g.cm²
Shaft Diameter (mm)	8mm
Motor Weight (kg)	0.9Kg
Motor Body Length L (mm)	58mm

Motor Driver and Nema24 motor

The motor driver acts as an intermediary between the microcontroller and the motor. Nema24 will ultimately be utilized as the device motor.

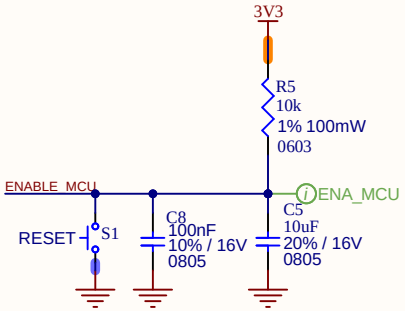
Designer's signature

Supervisor's signature

Sheet title: Motor Driver and Nema24 motor		
Project title: plunger_07.PrjPcb		
Desginer: Juan Alberto Serrano Redondo		
Date: 22/10/2024	Revision: 0.7	Sheet 15 of 15

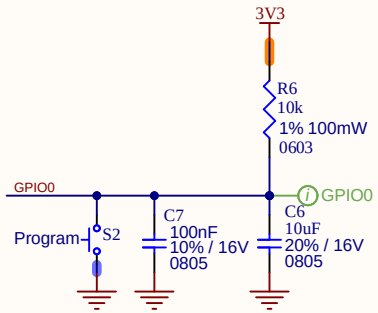
Supervisor:
Sr. Andrés Roldán Aranda
Dpto. Electrónica y Tecnología de Computadores
University of Granada
C/ Fuente Nueva, s/n, 18001
Granada, Granada, Spain

Reset



To ensure power stability to the microcontroller during powerup, this RC filter introduces a delay on the ENABLE pin. Usual values are 10 kΩ, 1 µF (τ = 10 ms, t_{10-90} = 22 ms). [ESP32-WROOM-32D datasheet, page

Boot mode selection (debug)



Allows to force 'Download' boot

Same design as in ESP32 DevKit boards.
100 nF cap are for debouncing and

Reset and programming buttons

Some of the buttons are meant for debugging like boot mode selection and reset, and will not be accesible to the end user.

Designer's signature

Supervisor's signature

Sheet title: Reset and programming buttons		
Project title: plunger_07.PrjPcb		
Desginer: Juan Alberto Serrano Redondo		
Date: 22/10/2024	Revision: 0.7	Sheet 16 of 17

Supervisor:
Sr. Andrés Roldán Aranda
Dpto. Electrónica y Tecnología de Computadores
University of Granada
C/ Fuente Nueva, s/n, 18001
Granada, Granada, Spain

TPS54540BQDDARQ1

FB pin regular voltage value is 0.8V.
To calculate the maximum switching frequency limitation set by the minimum controllable on time and the input to output step down ratio we use the following ecuations:

$$f_{SW(max\,skip)} = \frac{1}{t_{ON}} \times \left(\frac{I_O \times R_{dc} + V_{OUT} + V_d}{V_{IN} - I_O \times R_{DS(on)} + V_d} \right)$$

$$f_{SW(shift)} = \frac{f_{DIV}}{t_{ON}} \times \left(\frac{I_{CL} \times R_{dc} + V_{OUT(sc)} + V_d}{V_{IN} - I_{CL} \times R_{DS(on)} + V_d} \right)$$

$$f_{SW(max\,skip)} = \frac{1}{135ns} \times \left(\frac{1.5A \times 10.3m\Omega + 12V + 0.52V}{24V - 1.5A \times 92m\Omega + 0.52V} \right) = 3.8MHz$$

$$f_{SW(shift)} = \frac{8}{135ns} \times \left(\frac{6.3A \times 10.3m\Omega + 0.1V + 0.52V}{24V - 6.3A \times 92m\Omega + 0.52V} \right) = 1.7MHz$$

It's needed an output voltage of 12V and an output current of 1.5A with 24V of input voltage, the rest of the values have been taken from the device datasheet.
The switching frequency of the TPS54540-Q1 device is adjustable over a wide range from 100 kHz to 2500 kHz by placing a resistor between the RT/CLK pin and GND pin. The RT/CLK pin voltage is typically 0.5 V, and must have a resistor to ground to set the switching frequency.

$$R_T\ (k\Omega) = \frac{101756}{f\text{sw (kHz)}^{1.008}}$$

$$f\text{sw (kHz)} = \frac{92417}{RT\ (k\Omega)^{0.991}}$$

$$R_T(k\Omega) = \frac{101756}{400^{1.008}} = 242k\Omega$$

For this design, a lower switching frequency of 400 kHz is chosen to operate comfortably below the calculated maximums.

The voltage divider of R5 and R6 sets the output voltage.
Due to the input current of the FB pin, the current flowing through the feedback network should be greater than 1 µA to maintain the output voltage accuracy. This requirement is satisfied if the value of R6 is less than 800 kΩ. Choosing higher resistor values decreases quiescent current and improves efficiency at low-output currents but may also introduce noise immunity problems.

$$R_{HS} = R_{LS} \times \frac{12V - 0.8V}{0.8V}$$

With 10kΩ as the value for RLS we need a RHS of 140kΩ to have an output of 12V.

24V to 12V DCDC converter specifications

Specifications and parameters for designing a dc-dc converter are identified.
All auxiliary component values can be obtained from the device datasheet.

Designer's signature

Supervisor's signature

Sheet title: 24V to 12V DCDC converter specifications		
Project title: plunger_07.PrjPcb		
Desginer: Juan Alberto Serrano Redondo		
Date: 22/10/2024	Revision: 0.6	Sheet 17 of 17

Supervisor:
Sr. Andrés Roldán Aranda
Dpto. Electrónica y Tecnología de Computadores
University of Granada
C/ Fuente Nueva, s/n, 18001
Granada, Granada, Spain