IEEE STANDARDS

IEEE Recommended Practices #P1485 on:

Test Procedures for

Micro-electronic MOSFET Circuit Simulator Model Validation

(Working Draft - completed 05/21/97)

Contents:

1. Overview

This recommended practice is divided into 6 clauses. Clause 1 provides the scope of this recommended practice. Clause 2 provides definitions that are useful to understanding and applying this recommended practice. Clause 3 provides two tables and a list for cross referencing the tests, characteristics, and applications of the devices specified in this recommended practice. Clause 4 shows the test procedure description. Clause 5 lists the qualitative tests and describes their importance. Clause 6 describes the quantitative tests.

This recommended practice also contains 3 annexes. Annex A contains a list of figures and list of tables. Annex B contains a bibliography. Annex C contains netlists to perform the recommended tests.

1.1 Scope

This is a recommended practice for comprehensive test procedures for validation of micro-electronic MOSFET models that are used with circuit simulators. The procedures are to validate the models as to their external terminal behaviour only.

2. Definitions

For the purposes of this recommended practice, the following terms and definitions apply [B1][1]. The IEEE Standard Dictionary of Electrical and Electronics terms should be used for terms not defined in this section.

[1]The numbers in the brackets correspond to those of the bibliography in Annex B.

2.1 compact model

A compact model is a set of equations and parameters for those equations to be used in a SPICE-like simulator.

2.2 I_d

The drain current of a micro-electronic MOSFET.

2.3 Voltages and reference

V_{ds} is the drain to source voltage working in a source-referenced framework. Similiarly, V_{bs} is the bulk to source voltage and V_{gs} is the gate to source voltage. In a bulk-referenced framework, V_{db} would be the drain to bulk voltage, V_{gb} the gate to bulk voltage, and V_{sb} the source to bulk voltage. Note, the subscripts d, g, s, b are denoted as drain, gate, source, and bulk respectively.

2.4 TH characteristics

These characteristics are called the threshold characteristics of a micro-electronic MOSFET. Normally, these entail a plot of I_d versus V_{gs} over V_{bs} for one or more values of V_{ds}.

2.5 ST characteristics

These characteristics are called the subthreshold curves of a micro-electronic MOSFET. These curves are plots of $\log(I_d)$ versus V_{gs} near threshold over V_{ds}, for one or more values of V_{bs}.

2.6 TS characteristics

These characteristics are called the triode-saturation or output characteristics of a micro-electronic MOSFET. These curves are defined as I_d versus V_{ds}, over V_{gs}, for one or more values of V_{bs}.

2.7 I_{sat}

This is the saturation current, defined as I_d with V_{db} and V_{gb} equal to the supply voltage (V_{dd}).

2.8 V_{diode}

This is defined as V_{db} when

$V_{db}=V_{gb}$ and $I_d=0.1uA \times (W_d/L_d)$,

where
W_d and L_d are the designed dimensions of the micro-electronic MOSFET.

2.9 L_m, W_m, L_{max}, W_{max}, W_{min}, L_{min}, L_{eff}, W_{eff}

These are the MOSFET dimensions. The ***m*** subscript is for masked size, ***max*** subscript is for the largest size, ***min*** subscript is for the minimum allowable size, and ***eff*** subscript is for the effective size.

2.10 DIBL

This is defined as the drain induced barrier lowering (the decrease in V_{gs} needed to maintain a constand I_d below threshold, as V_{ds} is increased).

2.11 V_{tv}

This is the thermal voltage, defined as

(K x T)/q

where
K is Boltzmann's constant,
T is temperature in K
q is the magnitude of the electronic charge.

2.12 V_{th}

This is the threshold voltage of the micro-electronic MOSFET.

3. Model Application Classification

This section correlates the test names to the specific device characteristics. It also shows the device applications where the test coverage is required. All of the applications listed have a number of corresponding tests and device features that are important for that application.

3.1 List of device applications

1. Digital circuits
2. Analog circuits
3. Memory circuits
4. RF circuits
5. High speed circuits
6. Low voltage circuits
7. Mixed analog/digital circuits

3.2 Table 1 - Characteristics/applications cross-reference

Table 1 lists the applications that are associated with each device characteristic [B1].

Table 1 - Characteristics/applications cross-reference	
Device characteristics	Application Number
a.) Short channel effects	1,2,3,5,6,7
b.) Mobility effects	1,2,4,5,7
c.) Substrate effects	2,3,4,6
d.) IV characteristics	1 - 7
e.) CV characteristics	1 - 7
f.) Moderate inversion	2,6,7
g.) Smooth and continuous derivatives	2,4,5,6,7
h.) Symmetry	1,3,5,7
i.) R_{out} characteristics	2,7
j.) Non-quasi-static behaviour	2,4,7

k.) Noise	2,4,5,7
l.) Scaling of devices	1,3,6

3.3 Table 2 - Tests/characteristics cross-reference

Table 2 shows the tests that are associated with each device characteristic [B1].

Table 2 - Tests/characteristics cross-reference	
Test	Characteristic letter
TS characteristics I_d and g_o	a,b,d,g
TH characteristics I_d and g_m	a,b,d,g
ST characteristics, log(I_d) and g_m	a,b,c,d,g
Tsvidis/Suyama Tests 1-6 [B2]	f,g,i,j,k
I_{sat} and V_{diode} over T and V_{sb} for short and long devices	d,l
I_{sat} x L_m and V_{diode} over L_m	d,l
I_{sat}/W_m and V_{diode} over W_m	d,l
Fine grid tests (V_{gb} and V_{db}) - 3 tests	g
log(g_o) over I_d	f,g
Gummel tests - 3 tests	g,h
Capacitance fine grid tests - 2 tests	e

4. Test procedure

The test procedure consists of several tests of the model itself (without fitting any measured data) and similar tests where the model is shown after fitting to data and the relative errors are recorded.

This recommended practice does not cover test structures for the measurements or the test equipment, software, or platform for the data acquisition. The recommended practice will treat the micro-electronic MOSFET device as a four terminal device, with the terminals defined in the Definitions clause (clause 2.3).

The tests are seperated into two catagories, qualitative and quanitative. The qualitiative tests are used to determine the micro-electronic MOSFET model capabilities and to show any short comings in the model equations. Default model parameters should be used for these tests. The quanitative tests are performed to show the model accuracy with an fitted parameter set. These tests will show how accurately a model can electrically represent a fabricated device. Error percentages should be noted. The actual allowable error from model to measured data is not specified, as different applications will have different acceptable errors.

5. Qualitative tests

This section of the recommend practice describes the qualitative tests for the micro-electronic MOSFET model [B1]. These tests should be performed on the model before the quanitative tests are performed. Any anomolies should be

recorded and reported to the model developer.

5.1 Table of model capabilities

The first step toward model valadation is to determine the basic properties of the micro-electronic model. A convienent way of documenting such features is to use a table of model capabilities. An example is shown in table 3.

Table 3 - Table of model capabilities

Function	Capability
DC analysis	Yes
Transient analysis	Yes
AC analysis	Yes
Noise analysis	Yes
AC modeling basis	(Charge or capacitance)
Overlap/fringing capacitance modeling	(Bias dependent or independent
Drain/source-bulk depletion capacitance	Area and perimeter components
Drain/source-bulk junction current	Area and perimeter, forward and leakage components
Geometry dependence	Over length, width, and source/drain geometry
Temperature dependence	Yes
Model basis	(Single piece or regional model)
Channel model	(Symmetric or asymmetric)
Drain/source parasitics	(Symmetric or asymmetric)
Reliability/degradation model	Yes
Substrate current model	Yes
Supports binning	(No or yes)
Parameter extraction available	Yes

Note: The list of functions and possible responses will become larger as technologies advance. Current capabilities are shown.

5.2 TS characteristics I_d and g_o

This test comprises playbacks of TS (output) characteristics of a model, for wide/long and wide/short devices. The playbacks are for V_{sb}=0 and V_{sb}=V_{dd}, V_{gs}=V_{th} -0.15, V_{th}, V_{th} +0.15, and 3 values of V_{gs} equally spaced between V_{th} and V_{dd}, and V_{ds} swept from 0 to V_{dd} in 0.05 volt steps. Both I_d and g_o should be plotted, on linear and logarithmic ordinate scales.

A good model will show smooth transitions from triode to saturation regions, no regions of negative g_o, no kinks, glitches or discontinuities, and will have the rate of increase of g_o with V_{ds} increase as V_{sb} increases. The output conductance should be higher, and saturation should occur at lower V_{ds}, for the short device than for the long device.

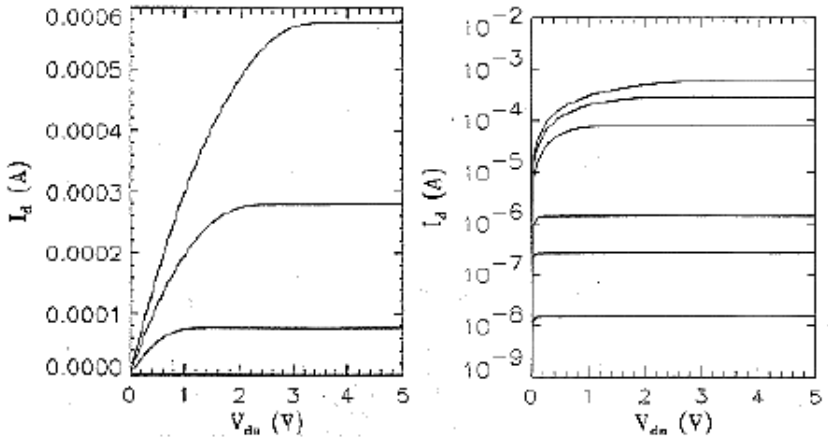

Figure 1: TS characteristics I_d (log and linear scale)

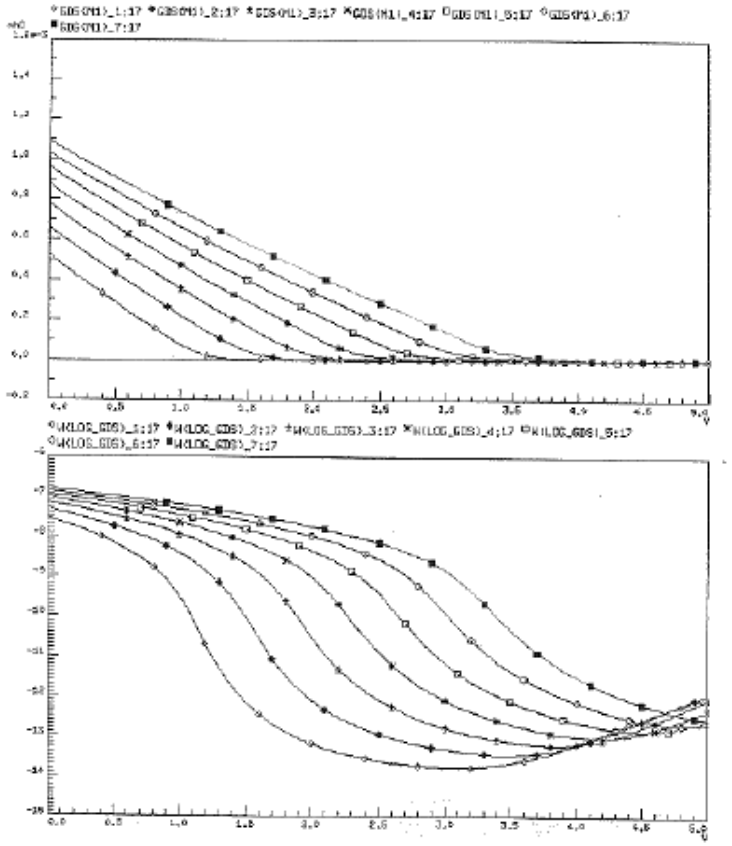

Figure 2: TS characteristics g_o (log and linear scale)

5.3 TH characteristics I_d and g_m

This test comprises playbacks of TH (threshold) characteristics of a model, for wide/long, wide/short, and narrow/long devices. The playbacks are for V_{ds}=0.1, V_{sb}=0, V_{dd}/2, and V_{dd}), and V_{gs} swept from 0 to V_{dd} in 0.05 volt steps. Both I_d and g_m should be plotted, on a linear ordinate scale.

A good model will show smooth transitions from below to above threshold, with no kinks, glitches or discontinuities. The peak g_m should decrease with increased V_{sb} for the wide/long device, and should not decrease as fast, or actually increase, with V_{sb} for the wide/short device. The relative curvature in the I_d curves should be greatest for the wide/short

device, less pronounced for the wide/long device, and least for the narrow/long device.

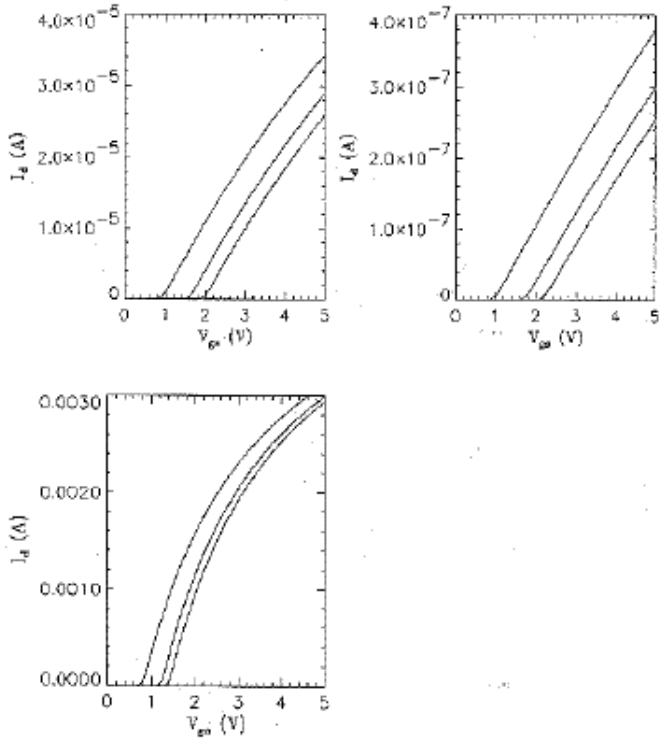

Figure 3: TH characteristics I_d

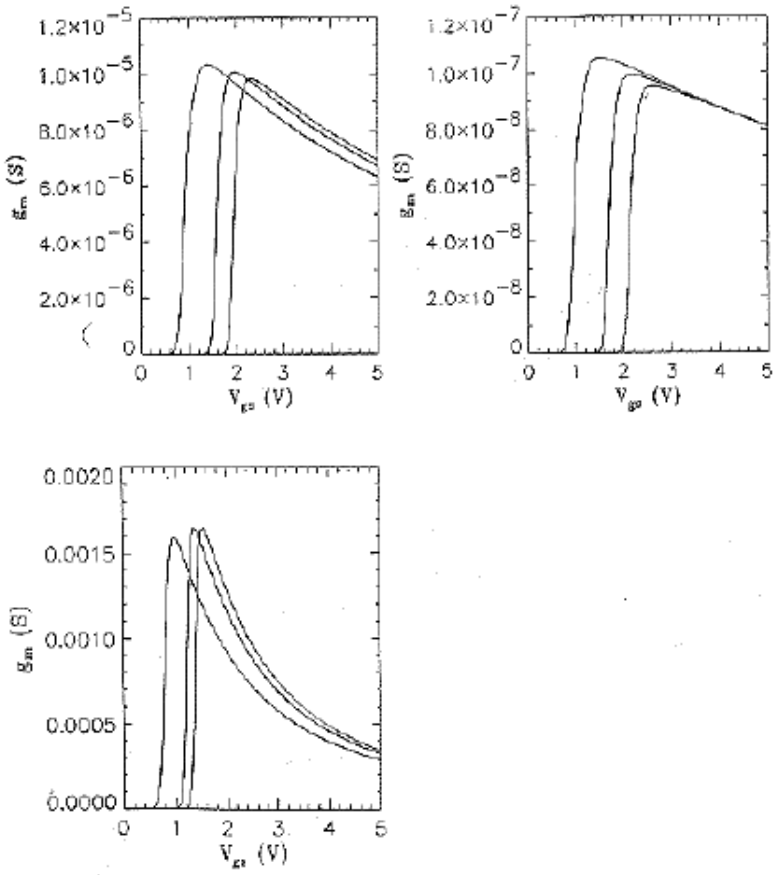

Figure 4: TH characteristics g_m

5.4 ST characteristics, log(I_d) and g_m

This test comprises playbacks of ST (subthreshold) characteristics of a model for the full range of devices. The preferred plotting would be log(I_d) versus V_{gs} near threshold for multiple V_{bs} values. The linear plot of the same data does not readily detect errors in the transition regions of micro-electronic MOSFET models.

A good model will show smooth transitions, with no kinks, glitches or discontinuities. The rolloff in log(I_d) should be smooth from high V_{gs} to low V_{gs}. Higher V_{bs} values should show higher values for log(I_d) until flattening occurs near V_{gs}<=V_{th}.

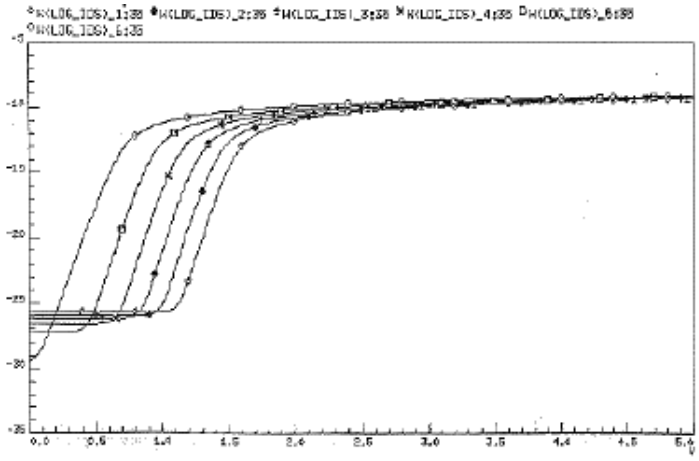

Figure 5: ST characteristics log(I_d) vs. V_{gs}

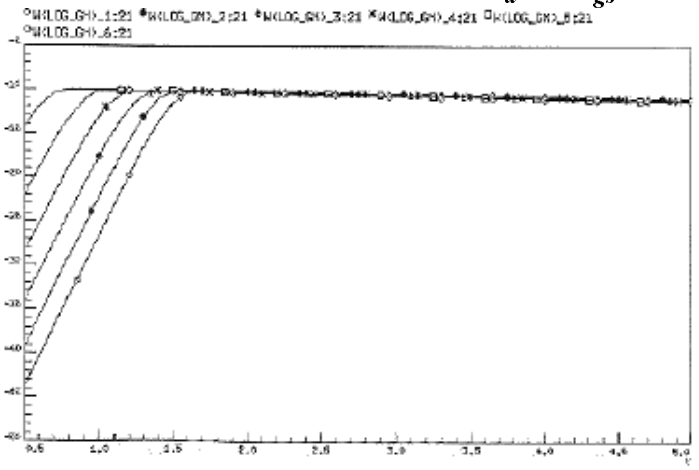

Figure 6: ST characteristics log(g_m) vs. V_{gs}

5.5 Tsvidis/Suyama Tests 1-6 [B2]

These tests show a micro-electronic MOSFET model's capability for analog design. Simple IV and CV curves are usually not enough to guarantee analog performance. These tests are considered a minimum starting point for analog performance.

1. For a V_{ds} value in the saturation region, plot I_d versus V_{gs}, with I_d on a logarithmic scale and including V_{gs} values well below threshold. The shape should be as illustrated in figure 1. The majority of the failures will be in the moderate inversion region of operation. This region has become more important as power supply voltages drop and device sizes shrink.

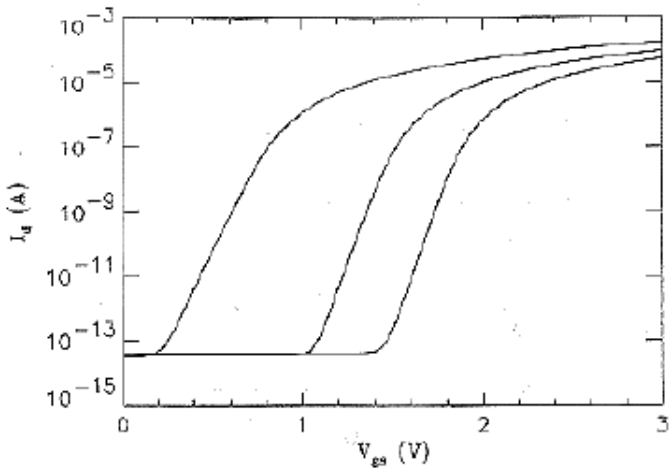

Figure 7: Moderate inversion I_d

2. Plot the transconductance-to-current ratio, g_m/I_d (an important quantity for analog design) versus V_{gs} or versus log (I_d) (same ranges as the test above). A good model should be smooth and continuous and give a shape similar to figure 2. Once again, the moderate inversion region will be the cause of modeling errors.

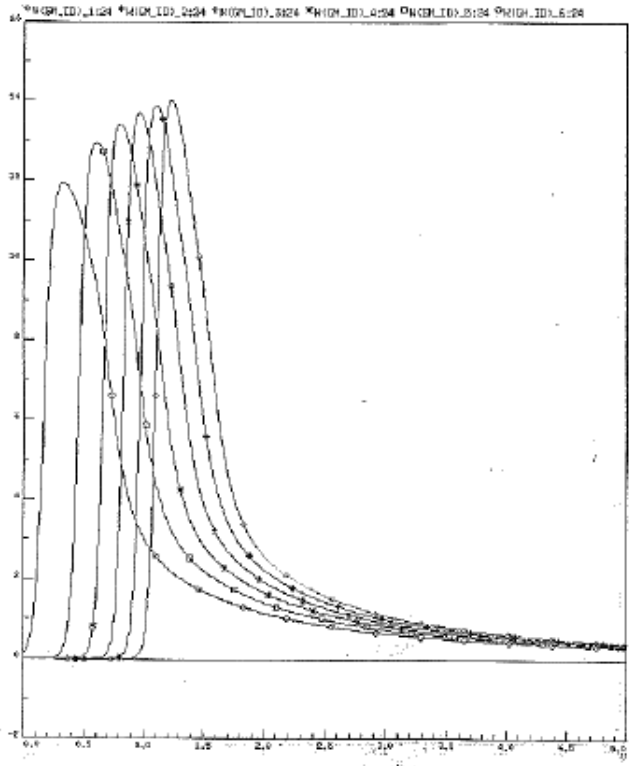

Figure 8: g_m/I_d test

3. Plot g_{ds} versus V_{ds} for a fixed value of V_{gs} (or for several values of V_{gs}). A good model will be smooth and continuous, showing no transition kinks or glitches for the triode to saturation transition.

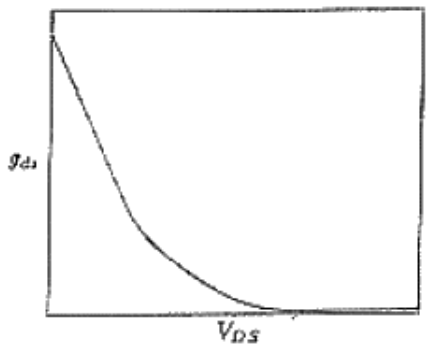

Figure 9: g_o test

4. Take the simplest form of the model possible (remove any parasitics for junction capacitance, overlap capacitance, series resistance, etc.) and do not specify an area or perimeter for the device in the device statement. Bias a 100um long MOSFET in strong inversion saturation. Use an AC source in series with the gate bias and obtain the frequency response for the drain current. Now, break the device into 2 - 50um long devices with their channels in series and with common substrate and common gate. The combination should be equivalent to the 100um device. Obtain the frequency response as with the 100um device, and the two should overlay. If not, the quasi-static approximation is being used in the MOSFET model. A good model should show a rolloff in the response that corresponds to the natural cutoff frequency of the transistor.

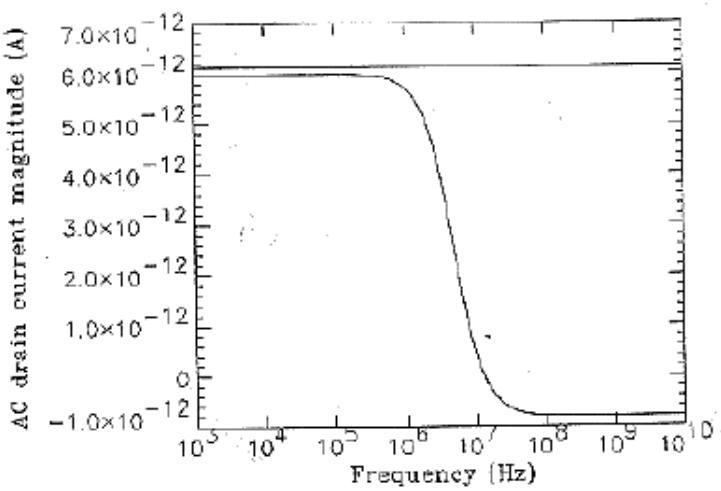

Figure 10: Frequency response test

5. Bias a device with a fixed V_{gs} in strong inversion and at a V_{ds} =0 (by placing a zero value DC current source between the drain and source). Run a noise simulation, for a frequency low enough so that the result is not affected by the intrinsic capacitances. Biased this way, the channel is a resistor of value $R = 1/g_{ds}$ and should show a thermal noise voltage with power spectral density of

   $4 \times K \times T \times R$

   where
   K is Boltzmann's constant
   T is temperature in K
   $R = 1/g_{ds}$
   (approx. 1.66×10^{-16} for a g_{ds} of 10^{-4} A/V)

   A good model will show the appropriate value. If using a MOSFET as a resistor, any variation would give errors in the simulation.

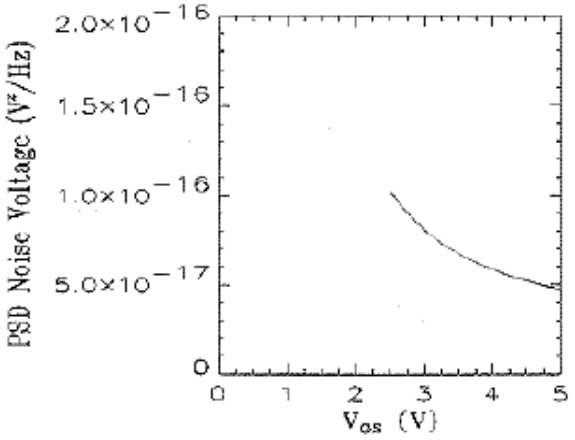

Figure 11: Resistive noise test

6. Bias a device in strong inversion saturation and run a noise simulation at frequencies where 1/f noise should be dominant. The noise current can be converted into a voltage across a 1 ohm resistor placed in series with the drain. Now, increase the channel width 10x. A good model will show the noise power spectral density to decrease 10x. Also, vary V_{gs} and the noise current should be insensative to the change.

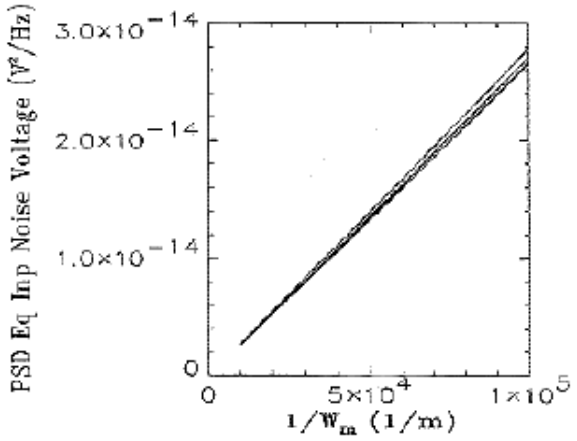

Figure 12: Noise width scaling test

5.6 I_{sat} and V_{diode} over T and V_{sb} for short and long devices

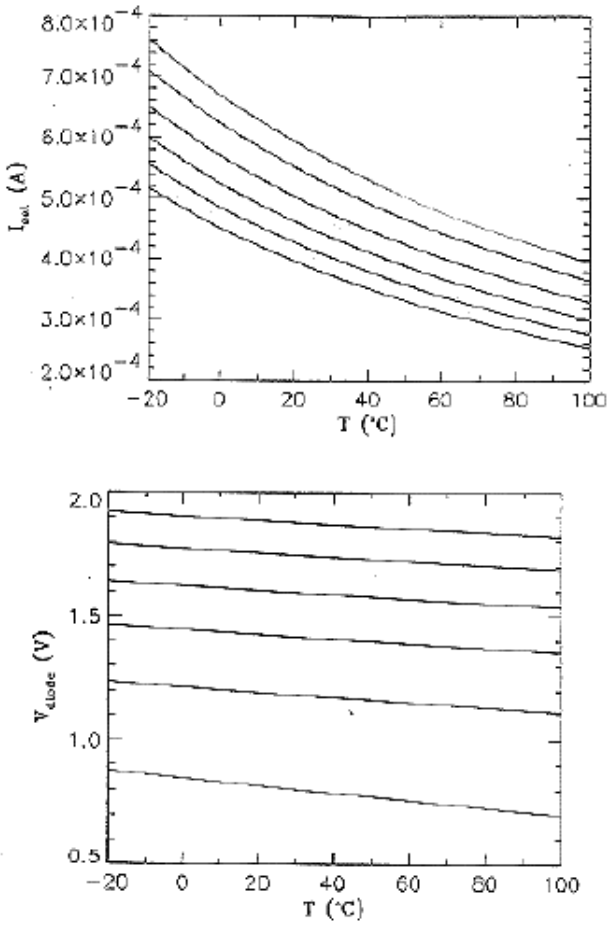

Figure 13: I_{sat} and V_{diode} vs. temperature (long device)

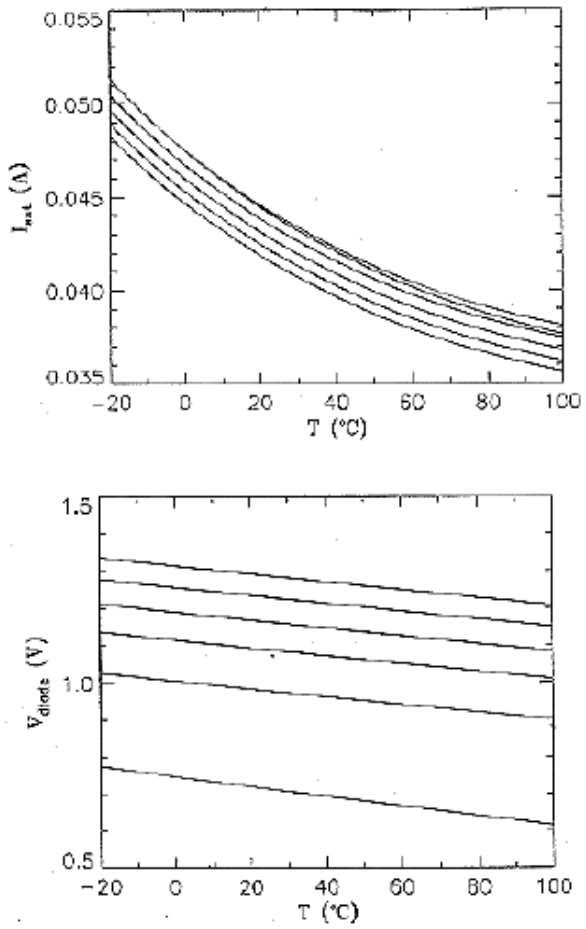

Figure 14: I_{sat} and V_{diode} vs. temperature (short device)

5.7 I_{sat} x L_m and V_{diode} over L_m

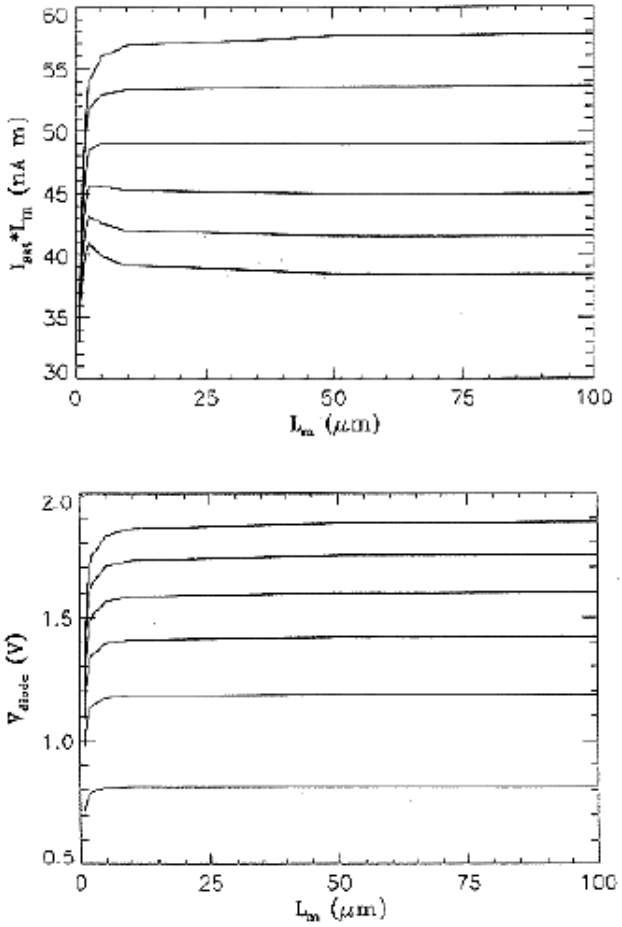

Figure 15: I_{sat} x L_m and V_{diode} vs. L_m

5.8 I_{sat}/W_m and V_{diode} over W_m

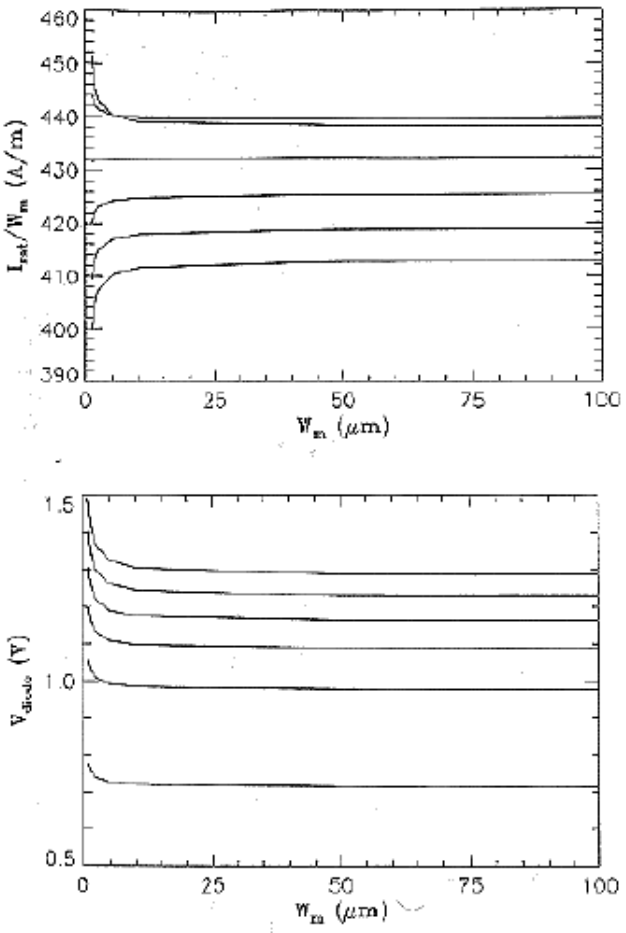

Figure 16: I_{sat}/W_m and V_{diode} vs. W_m

5.9 Fine grid tests (V_{gb} and V_{db}) - 3 tests

These tests are used to determine boundary transistions of regional models. When using a wider range of values for the voltages, micro-electronic MOSFET models may appear smooth and continuous. The only way to determine if a model is truly continuous is to check the model performance on a fine grid of voltage values.

1. ***Test of g_m over a fine V_{gb} grid***
   Commonly, playbacks of TH I_d and g_m characteristics using the same data spacing as for measurements have an insufficiently fine voltage grid to expose problems at boundaries between regions of a model. This test plots g_m, from TH data simulated with a 0.001 V_{gs} grid. The fine grid highlights problems in regional models at the boundary between below and above threshold operation. The plots should be done at V_{ds}=0.1 and for several values of V_{sb}.

   A model fails this test if it does not have a smoothly peaked transition in g_m from below to above threshold. A model passes this test if it has a single, smooth peak in g_m, with no kinks or glitches.

2. ***Test of g_o over a wide range, fine V_{db} grid***

   Commonly, playbacks of TS I_d and g_o characteristics using the same data spacing as for measurements have an

insufficiently fine voltage grid to expose problems at boundaries between regions of a model. This test plots g_o, from TS data simulated with a 0.001 V_{ds} grid. The fine grid highlights problems in regional models at the boundary between below and above threshold operation. The plots should be done at several values of V_{gs}.

A model fails this test if it does not have a smoothly peaked transition in g_o from below to above threshold. A model passes this test if it has a single, smooth peak in g_o, with no kinks or glitches.

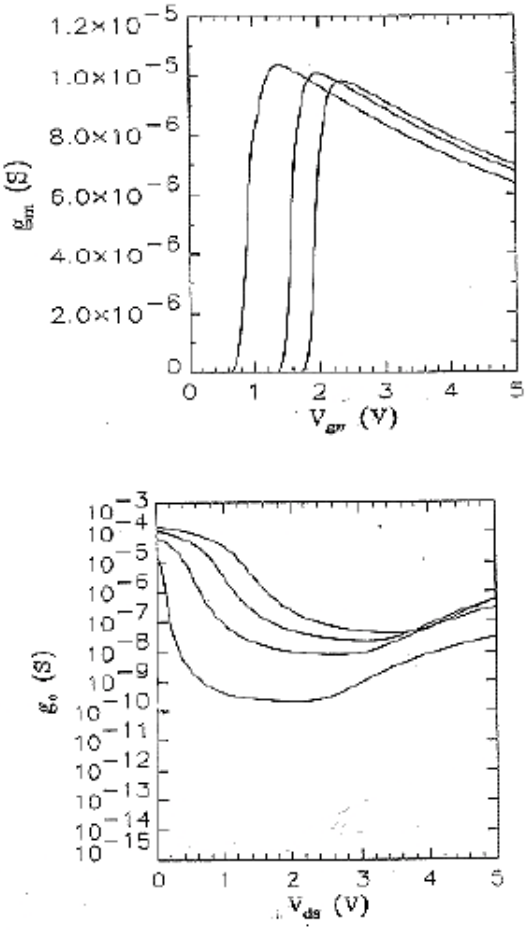

Figure 17: Fine grid tests for g_m and g_o

3. ***Test of g_o over a narrow range, fine V_{db} grid***

   This test is similar to the test above, but is done at one V_{gs} value over a narrow range of V_{ds} values around saturation. It is a magnified view of g_o near the saturation transition. A model passes this test if g_o smoothly decreases from triode to saturation region operation. A model fails this test if it has discontinuities, kinks or glitches at or near the saturation voltage.

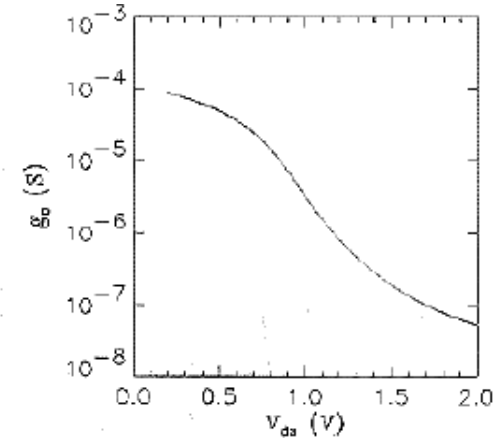

Figure 17b: Fine grid tests for g_o

5.10 log(g_o) over I_d

This test is another way of plotting data to highlight problems with regional models. For TS data from a fine V_{ds} grid, log (g_o) is plotted against log(I_d). The curves should be smooth, and as always devoid of kinks and glitches.

5.11 Gummel tests - 3 tests

For standard CMOS technologies, the MOSFETs are symmetric devices, in that the source and drain terminals can be labelled arbitrarily. Some devices are asymmetric by design, e.g. high power MOSFETs, and asymmetric operation of devices that were manufactured to be symmetric can cause asymmetries. However, a majority of MOSFET models are derived for the case of symmetric source and drain, and therefore should be symmetric. The tests described below are intended to show the symmetrical behaviour of a model.

1. ***Gummel symmetry test***
   If a MOSFET model is not symmetric, and is formulated explicitly for V_{ds} >0 and then has the terminal labelling switched if necessary during evaluation, it can lose continuity in high order derivatives at V_{ds}=0. This causes modeling inaccuracies, especially for pass transistors, and can cause problems for algorithms used in circuit simulation. This test shows if a model has a break in symmetry of I_d at V_{ds}=0.

   A MOSFET can be driven symmetrically by a single supply if it is biased with V_{gb} gate bias and with V_{sb}=V_{sb0}-V_x and V_{db}=V_{sb0}+V_x, where V_{sb0} is the initial (nonzero) drain- and source-to-bulk bias, and V_x is a single independent voltage source. I_d must be an odd function of V_x,

   $I_d(V_x) = -I_d(-V_x)$

   and this requires that all even order derivatives of I_d with respect to V_x be zero at V_{ds}=0. In particular

   $D^2I_d/DV_x^2 \mid_{Vx=0} = 0$

   Note: "D" is used as a symbol for the partial derivative

   must hold.

   A simple plot of $I_d(V_x)$ is insufficient to show if a model is properly symmetric in $I_d(V_x)$ or not. By plotting

$g_X=DI_d/DV_X$, both on a large scale and on a fine grid about $V_X=0$, the symmetry, or lack thereof, can be visualized.

A model fails this test if there is a discontinuity in the derivative of the curve of g_X at $V_X=0$. A model passes this test if g_X smoothly and continuously varies from negative to positive V_X, with a slope of zero at $V_X=0$.

Asymmetric models are typically those that are derived referenced with respect to the source, rather than to the bulk or gate. Although any MOS model can be arbitrarily referenced to any 3 of the 4 terminal voltages [B3], with the fourth as the reference, typically only bulk referenced models, such as charge sheet models, [B4] exhibit the proper symmetry.

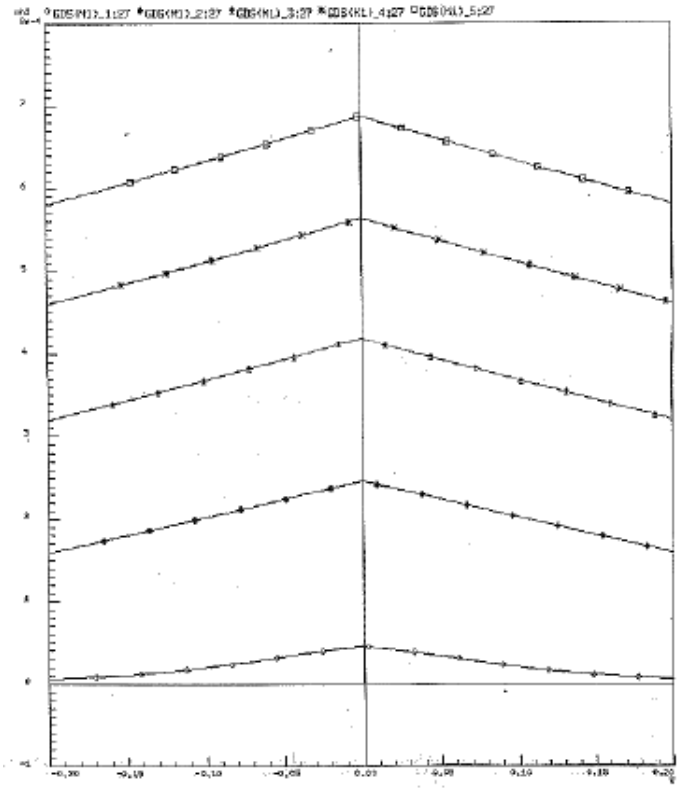

Figure 18a: Gummel symmetry test

2. ***Gummel slope ratio test***

Asymptotic behavior for low V_{ds} operation can be well approximated by simple theoretical models. This leads to a simple and useful aid to evaluate whether a MOSFET model exhibits behavior dictated by fundamental device physics.

Consider two points, $I_1=I_d(V_{db}=V_1)$ and $I_2=I_d(V_{db}=V_2)$ from two small values V_1 and V_2 of V_{db}, for small V_{db} and $V_{sb}=0$. Typically, these points are the first two non-zero points on an output, or TS, curve. The slope ratio S_R is defined as

$$S_R = ((I_2 + I_1) \times (V_2-V_1)) / ((I_2-I_1) \times (V_2 + V_1))$$

and is the ratio of the slope of the line through the origin and the midpoint of the line connecting (V_1,I_1) and (V_2,I_2) to the slope of the line joining (V_1,I_1) and (V_2,I_2).

For large V_{gb}, operation is in the triode, or linear region, and I_d is close to linear in V_{db}, so S_R should approach unity. For small V_{gb}, in subthreshold operation, I_d is nearly proportional to $1-e^{(-V_{ds}/V_{tv})}$. S_R should thus reach an

asymptote that is determined by the temperature and the values of V_1 and V_2.

A model passes this test if it approaches the expected asymptotes. A model fails this test if it does not approach the asymptotes, and if it displays kinks and glitches in the S_R curve.

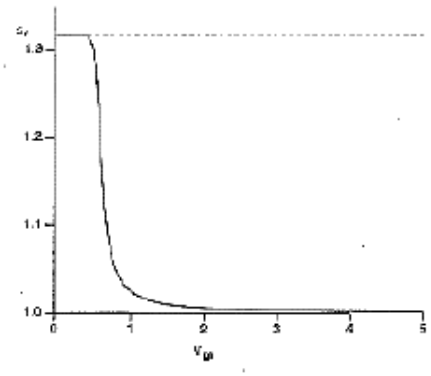

Figure 18b: Gummel slope ratio test

3. ***Gummel treetop curve test***

The so-called subthreshold slope is an important measure of MOSFET performance, and lends itself to testing asymptotic behavior of MOSFET models. This test examines how a model agrees with expected theoretical behavior.

For a long channel MOSFET with a uniformly doped substrate, to a good approximation

$$I_d = (u_0 \times C_{ox} \times (W/L)) \times (0.5 \times (Gamma) \times V_{tv}^2 / (Sqrt((Psi)_{sa})) \times e^{(((Psi)_{sa} - (2 \times (Phi)_F) - V_{sb}) / V_{tv}) \times (1 - e(-V_{ds}/V_{tv}))}$$

holds, where

$$(Psi)_{sa} = (-0.5 \times (Gamma) + (Sqrt((0.25 \times (Gamma)^2 + V_{gb} - V_{fb})))^2$$

It follows that

$$Dlog(I_d)/DV_{gb} = g_m/I_d = (1/V_{tv} - 0.5/(Psi)_{sa}) D(Psi)_{sa}/DV_{gb}$$

Note: "D" is used as a symbol for the partial derivative

This shows that g_m/I_d should asymptotically reach a value that depends on V_{gb} in subthreshold operation, and that for large V_{gb} the value approaches $1/V_{tv}$, the reciprocal thermal voltage. The correct asymptotic behavior is apparent, as is the reason for naming this the treetop plot.

Note that the physical theory underlying this test assumes a uniformly doped channel. This means behavior for real devices can vary slightly from the predicted ideal behavior. Also note that junction leakage at low currents causes significant differences between actual and theoretical values, and that shunt conductances g_{min} in circuit simulators can also introduce artifacts into g_m/I_d at low currents. The junction leakage and g_{min} effects need to be excluded from data used for this test. Despite these caveats, the theoretical behavior is observed in practice in nonuniformly doped, long channel MOSFETs. For short channel devices, the asymptotic treetop curve is approached but not reached.

A model passes this test if it closely follows the treetop curve for subthreshold operation, and if it does not display any kinks or glitches. A model that does not approach the treetop curve fails this test, and that include models with constant g_m/I_d values. Simple subthreshold models that depend exponentially on V_{gs}-V_{th} will have a constant

g_m/I_d in subthreshold operation, often independent of V_{sb}, and so fail this test. Note that in the microelectronics vernacular "subthreshold slope" is a commonly used quantity. In fact, there is no region of constant g_m/I_d, and so the concept that underlies this quantity is inaccurate.

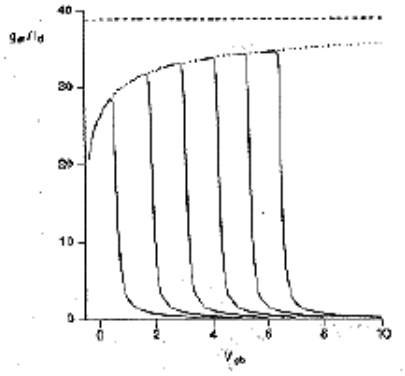

Figure 18c: Gummel treetop curve test

5.12 Capacitance fine grid tests - 2 tests

Capacitances are as important as I_d and conductance modeling for both digital and analog circuits. However, there has been much less emphasis on MOSFET charge and capacitance modeling in MOSFET modeling. Consequently understanding of weaknesses of charge and capacitance models is less widespread than for DC current modeling. These two tests involve plotting and inspection of MOSFET capacitances.

MOSFET capacitance coefficients can be viewed in two ways. The most direct and physically based is to directly consider how they affect MOSFET terminal currents. For small-signal AC behavior, the (complex valued) current flowing into node i of the transistor is

$I_i = \boldsymbol{E}_k (g_{ik} + j \times (\text{Omega}) \times C_{ik}) \times V_k$

where the summation is over all terminals k, V_k is the AC voltage exciting terminal k, g_{ik} and C_{ik} are the conductance and capacitance coefficients relating I_i to V_k, Omega is frequency (radians per second) and j is Sqrt(-1). From this the definition of C_{ik} is, for V_k=1+j0 and all other AC excitations being zero

$C_{ik} = \lim((\text{Omega})\text{--}> 0)\ \text{Im}(I_i)/(\text{Omega})$

This is a consistent definition of capacitance coefficients in terms of low frequency AC terminal measurements. This definition readily lends itself to evaluation of C_{ik} in a circuit simulator. By sequentially AC exciting all terminals with a voltage 1+j0, all other AC terminal biases being zero, and doing an AC analyses at Omega=1, $\text{Im}(I_i)$ can be directly printed for all nodes, giving the capacitance coefficients. These are the coefficients as seen by the simulator, including any errors in derivatives and stamping, and so they better represent how a model will behave for real circuit simulations than capacitances coefficients printed directly from model code.

A more convenient way to look at capacitance coefficients for MOSFETs is as the derivative of charges [B5]

$C_{ik} = -DQ_i/DV_k$, (i is not equal to k)

Note: "D" is used as a symbol for the partial derivative

In this view, only 3 independent charges are needed to view the 9 independent MOSFET capacitance coefficients, which simplifies modeling.

1. ***Gate capacitances over a fine V_{gb} grid***
   This test plots C_{gs}+C_{gd}, C_{gb}, and C_{gg}=C_{gs}+C_{gd},+C_{gb} against V_{gs} for V_{ds}=0 and 1.5 and for V_{sb}=0 and V_{dd}. The V_{gs} grid should be fine, of order 0.01V, and should extend from -V_{dd} to V_{dd}. The plots should be done for long and short channel devices, and should be only for intrinsic MOSFET capacitances, and not include parasitic junction, overlap, and fringing capacitances.

   A model fails this test if it has discontinuities or distinct, abrupt boundaries in the capacitance coefficients, which typically occur at flatband and threshold. A good model has smoothly varying capacitance coefficients.

   The maximum capacitance in accumulation and strong inversion should be $L_{eff}W_{eff}C_{ox}$, where C_{ox} is the gate oxide capacitance per unit area. The "plateau" region above threshold for the V_{ds}=1.5 curve should be at 2/3 of this value for the long channel device, and at a proportion higher than 2/3 for the short channel device.

2. ***Gate capacitances over a fine V_{db} grid***
   As with the previous test, this test is designed to expose weaknesses in MOSFET capacitance modeling instead of analyzing some capacitances as functions of gate bias. This test plots a set of 9 independent capacitance coefficients as V_{ds} varies from 0 to V_{dd}, for V_{gs}=V_{dd} (so operation is in strong inversion) and V_{sb}=0. The 9 capacitance coefficients plotted are C_{gs}, C_{gd}, and C_{dg}; C_{bs}, C_{bd}, and C_{db}; and C_{gb}, C_{sd}, and C_{bg}. These capacitance coefficients should be plotted for a fine grid, spacing 0.001 to 0.01V, in V_{ds}. The plots should be done for a short and a long channel device.

   This test can expose many weaknesses of MOSFET charge/capacitance models. These are the aspects of the plots to evaluate. A MOSFET model for a symmetric device should be symmetric at V_{ds}=0. Therefore a model fails this test if C_{gs} is not equal to C_{gd} is not equal to C_{dg} or C_{bs} is not equal to C_{bd} is not equal to C_{db} at V_{ds}=0. For the long channel device C_{gs} should smoothly increase from $L_{eff}W_{eff}C_{ox}$/2 to 2$L_{eff}W_{eff}C_{ox}$/3 as V_{ds} increases from 0 to its saturation values V_{dsat}. Concomitantly C_{gd} should smoothly decrease from $L_{eff}W_{eff}C_{ox}$/2 to 0 C_{sd} should be negative at V_{ds}=0, and along with C_{db} should smoothly become zero for V_{ds} above V_{dsat}. There should be no discontinuities in any of the capacitance coefficients through V_{dsat}. Also, the V_{dsat} for the capacitance coefficients should be the same as the V_{dsat} for the TS characteristics for the same channel lengths.

   For the short channel device saturation should occur at a lower V_{ds} value, and C_{gs} should increase to a value above 2$L_{eff}W_{eff}C_{ox}$/3.

   Inconsistency between saturation in I_d and charge/capacitance modeling is a subtle problem and is exposed by this test.

6. Quantitative Tests

The quantitative tests evaluate how well a micro-electronic MOSFET model can model representative MOSFET characteristics [B1]. This requires data and a reasonable parameter extraction methodology. Data can come from both physical simulations and from measurements. Data for all of the quantitative tests should include W_{max}/L_{max}, W_{max}/L_{min}, W_{min}/L_{max} and W_{min}/L_{min} devices, and preferably a wide device with length 1.5 times L_{min} for a technology and a long device with width 1.5 times W_{min}. The data should be for a range of temperatures from -50C to 150C.

Note that the quantitative tests are more than just metrics of how well a model can fit a particular data set. Models with reasonable parameter values can quantitatively look reasonable, yet with parameters extracted to fit a particular data set deficiencies in a model (or a parameter extraction algorithm) can be uncovered. For this reason, applications of the quantitative tests should explicitly record the extraction program and version used, as well as the model and version.

6.1 Playback of TS characteristics, I_d and g_o

This test is the equivalent of the qualitative test 5.2, however instead of just inspecting the model curves, the fit of the model to data is relevant. The same criteria as apply to qualitative test 5.2 apply here, so models should exhibit neither distinct regional boundaries nor negative g_o, and should model I_d and g_o well both above threshold and near and below threshold. Output conductance (including impact ionization degradation at moderate gate bias and high drain bias) should be modeled accurately over geometry, and g_o for long devices should be modeled well.

6.2 Percent error in I_d and g_o for TS characteristics

This test plots the relative error in fits to devices of quantitative test 6.1. Fit metrics reported should include maximum magnitude absolute and relative errors in I_d and g_o modeling, average magnitude absolute and relative errors in I_d and g_o modeling, and RMS absolute and relative errors in I_d and g_o modeling. The errors may further be reported separately for gate biases above threshold and below threshold.

6.3 Playback of TH characteristics, I_d and g_m

This test is the equivalent of the qualitative test 5.3, however instead of just inspecting the model curves, the fit of the model to data is relevant. The same criteria as apply to qualitative test 5.3 apply here. $I_d$should be modeled accurately over geometry and V_{sb} (and have no crossing of curves over V_{sb}), and g_m should not exhibit distinct regional boundaries. The modeling should be good for I_d and g_m both above threshold and near and below threshold. The behavior of the peak g_m over V_{sb} and geometry should be modeled well, including the decrease in the drop in peak g_m over V_{sb}, and potential increase in this peak, as L_m decreases.

6.4 Percent error in I_d and g_m for TH characteristics

This test plots the relative error in fits to devices of quantitative test 6.3. Fit metrics reported should include maximum magnitude absolute and relative errors in I_d and g_m modeling, average magnitude absolute and relative errors in I_d and g_m modeling, and RMS absolute and relative errors in I_d and g_m modeling. The errors may further be reported separately for gate biases above threshold and below threshold.

6.5 Playback of ST characteristics, log(I_d) and g_m

This test is the equivalent of the qualitative test 5.4, however instead of just inspecting the model curves, the fit of the model to the data is relevant. The same criteria as apply to qualitative test 5.4 apply here. DIBL should be modeled well over V_{sb} and geometry, and subthreshold currents should be modeled accurately.

6.6 Percent error in I_d and g_m for ST characteristics

This test plots the relative error in fits to devices of quantitative test 6.5. Fit metrics reported should include maximum magnitude relative errors in I_d and g_m modeling, average magnitude relative errors in I_d and g_m modeling, and RMS

relative errors in I_d and g_m modeling.

6.7 Capacitance playback and error percentage

a. V_{gb} over V_{db} and V_{sb}
This test is the equivalent of qualitative test 5.12, however instead of just inspecting the model curves the fit of the model to data is evaluated. The model should smoothly and accurately fit the capacitances around flatband and threshold, and should obey the same criteria as qualitative test 5.12. In particular, it should model individual C_{gs}, C_{gd}, and C_{gb} components over bias and geometry, especially for short and narrow devices.

The percentage error portion of this test plots relative errors in fits to the data of the test above. Fit metrics should include maximum and average magnitude and RMS errors in modeling the components of gate capacitance over all biases.

b. Versus V_{bd}
This test is the equivalent of qualitative test 5.12, but again the fit of the model to data is important, as well as qualitative modeling characteristics. The model should accurately account for short channel effects (premature saturation and capacitance increase due to velocity saturation) and should be consistent in terms of saturation, over geometry, with the TS characteristics of quantitative test 6.2. There should be no discontinuities in capacitances, and C_{sd} should be negative. The capacitances C_{gs}, C_{gd} and C_{dg}, and the capacitances C_{bs}, C_{bd} and C_{db}, should be equal at V_{ds}=0, for a symmetric device.

The percentage error portion of this test plots relative errors in fits to the data of the test above. Fit metrics should include maximum and average magnitude and RMS errors in modeling the components of gate capacitance over all biases.

6.8 Playback of DIBL over channel length

This test evaluates the accuracy of modeling DIBL over channel length. DIBL is exquisitely sensitive to effective channel length L_{eff}, so errors in modeling either DIBL or L_{eff} are uncovered by this test. From data and from a model, the logarithm of DIBL, defined as (the magnitude of) the difference in V_{gs} needed to give the same drain current, 0.1uA x W_m/L_m, for V_{ds}=0.1 and V_{ds}=V_{dd}, is plotted against $1/L_m$. This test can be applied for V_{sb}=0 and V_{dd}. A model should accurately track the increase in DIBL as L_m decreases.

6.9 Playback of g_o over channel length

This test evaluates the accuracy of modeling g_o over channel length. Plot g_o, measured and simulated at V_{ds}=V_{gs}=V_{dd} and V_{ds}=V_{gs}=V_{dd}/2 (for both V_{sb}=0 and V_{dd} for both cases), against $1/L_m$. MOSFET models should accurately track the increase in g_o as L_m decreases.

g_o is an important parameter for analog modeling, and there is often a trade-off between speed and drive capability, pushing to short channel lengths, and high AC gain (and matching), pushing to long channel lengths. Accurate g_o modeling is necessary to allow such design trade-offs to be made properly.

Annex A

(informative)

A.1 List of tables

A.2 List of figures

Annex B

(informative)

Bibliography

[B1] McAndrew, C., McSwain, M. et al, "Benchmarks for compact MOSFET models", *SEMATECH Compact Models Workshop*, Sunnyvale, CA, August 11th, 1995. (Unpublished).

[B2] Tsvidis, Y., and Suyama, K. "MOSFET modeling problems for analog circuit CAD: Problems and prospects", *1993 IEEE Custom Integrated Circuits Conference Proceedings*, pp. 14.1.1-14.1.6, May, 1993.

[B3] Ihantola, H. and Moll, J., "Design Theory of a surface field-effect transistor", *Solid State Electronics*, vol. 7, pp.423-430, 1964.

[B4] Tsvidis, Y., *Operation and modeling of the MOS Transistor*, New York: McGraw-Hill, 1987.

[B5] Turchetti, C. and Tsvidis, Y., "On the small signal behaviour of the MOS transistor in quasi-static operation", *Solid State Electronics*, vol. 26, no. 10, pp.941-949, Oct. 1993.

Annex C

(informative)

This Annex contains a listing of HSPICE netlists for several of the benchmark tests. It is not a complete set, however, it does have most of the benchmark tests documented in this recommended practice.

```
This file contains a set of HSPICE test netlists intended to form the beginning
of a Sematech model QA test suite, notes on options and templates used, and
suggestions for improvement.

These tests are intended to help model developers and Sematech model evaluators
detect qualitative problems with a compact device model that would seriously
impair its chances of success as an industry standard model.  These tests by no
means form a complete model QA test suite; there is no such thing.  However,
each netlist contains comments about the object of each test, and it's usually
easier to modify an existing netlist than to start from scratch.  Single devices
are the target for these tests, not large circuits.

HSPICE allows the use of parameters and element printback templates, which
simplifies netlist creation considerably.  The HSPICE .measure statement was not
used in these tests.  It is assumed that users of other simulators will be able
to modify these netlists to run via a more 'vanilla' SPICE.

All of the netlists use a common set of options.  TNOM=27 sets the nominal
simulation temperature (HSPICE usually defaults to 25'C).  GMIN is set very
small to minimize the influence of shunt conductances upon simulation results.
NUMDGT is set high to print many significant digits.  OPTS prints out all of the
options in effect in a simulation.  POST=2 allows use of the MetaWaves GUI for
postprocessing.  NOPAGE saves paper.  Simulations which sweep capacitances in a
.DC simulation use the DCCAP option to force evaluation of capacitance equations
for the sweep.

Tolerances and many other options can be specified; the object is to test the
behavior of the device model with as much precision as possible.

The HSPICE .data statement was not used.  Values of sweep limits or initial bias
points were arbitrarily chosen and may need to be modified via such a statement.
Similarly, quantitative comparison of measured and modeled data is not included
in these tests, as different simulators may use different means of importing
data.  Awk or perl scripts can be written to help automate the model QA process,
but such scripts can be very simulator-dependent.

These tests are for NMOS devices only, but should be replicated for PMOS devices
as well.  A fully parameterized typical model called nch.mod is .INCLUDEd in
most netlists, though some require a model with no parasitic resistances in a
file called nornch.mod.  Arbitrary Level 28 models were used for initial netlist
functional evaluation.  These are not measurement-based Meta Labs models.

The name mtest1.sp was reserved for a summary table of model features, which has
not yet been developed.  Note that mtest13.sp is incomplete at this time.

Thanks to Colin McAndrew, H. K. Gummel, Bill Scott, Yannis Tsividis, and Ken
Suyama for test ideas.  Anyone with additional ideas for test netlists should
submit them (or test netlists) to the Sematech model quality assurance /
benchmarking group.

*MTEST2 OUTPUT CHARACTERISTICS TEST
```

```
*HSPICE SEMATECH MODEL QA NETLIST
*The object of this test is to check the output characteristics of a device.
*Id, go, and 1/go are plotted against Vds.
.OPTION TNOM=27 GMIN=1E-14 NUMDGT=9 OPTS POST=2 NOPAGE
.WIDTH OUT=80
.INCLUDE 'nch.mod'
M1 1 2 3 4 nch
VD 1 5 DC 1
VG 2 6 DC 1
VS 3 7 DC 0
VB 4 8 DC 0
VDSENSE 0 5 DC 0
VGSENSE 0 6 DC 0
VSSENSE 0 7 DC 0
VBSENSE 0 8 DC 0
.OP
.DC VD 0 1 1E-3 VG 0 1 .1
.PRINT DC I(VDSENSE) lx8(M1) x=par('1/lx8(M1)')
*         ID         go      1/go
.END

*MTEST3 THRESHOLD CHARACTERISTICS TEST
*HSPICE SEMATECH MODEL QA NETLIST
*The object of this test is to check the threshold characteristics of a device.
*Id and gm are plotted against Vgs.
.OPTION TNOM=27 GMIN=1E-14 NUMDGT=9 OPTS POST=2 NOPAGE
.WIDTH OUT=80
.INCLUDE 'nch.mod'
M1 1 2 3 4 nch
VD 1 5 DC 1
VG 2 6 DC 1
VS 3 7 DC 0
VB 4 8 DC 0
VDSENSE 0 5 DC 0
VGSENSE 0 6 DC 0
VSSENSE 0 7 DC 0
VBSENSE 0 8 DC 0
.OP
.DC VG 0 4 2E-3
.PRINT DC I(VDSENSE) lx7(M1)
*         ID         gm
.END

*MTEST4 SUBTHRESHOLD CHARACTERISTICS TEST
*HSPICE SEMATECH MODEL QA NETLIST
*The object of this test is to check the subthreshold characteristics of a
*device.  log(Id) is plotted against Vds.
.OPTION TNOM=27 GMIN=1E-14 NUMDGT=9 OPTS POST=2 NOPAGE
.WIDTH OUT=80
.INCLUDE 'nch.mod'
M1 1 2 3 4 nch
VD 1 5 DC 3
VG 2 6 DC 1
VS 3 7 DC 0
VB 4 8 DC 0
VDSENSE 0 5 DC 0
VGSENSE 0 6 DC 0
VSSENSE 0 7 DC 0
VBSENSE 0 8 DC 0
.OP
.DC VD 0 4 1E-3
.PRINT DC I(VDSENSE) x=par('log(I(VDSENSE))')
*         ID         log(ID)
.END
```

```
*MTEST5 ISAT VS. TEMPERATURE AND VSB TEST
*HSPICE SEMATECH MODEL QA NETLIST
*The object of this test is to check Isat (Id when Vdb=Vgb=Vdd) versus
*temperature and Vsb, for short and long devices.
.OPTION TNOM=27 GMIN=1E-14 NUMDGT=9 OPTS POST=2 NOPAGE
.WIDTH OUT=80
.INCLUDE 'nch.mod'
.PARAM LENG=0.5E-6
M1 1 2 3 4 nch L=LENG W=1.0E-6
VD 1 5 DC 5
VG 2 6 DC 5
VS 3 7 DC 0
VB 4 8 DC 0
VDSENSE 0 5 DC 0
VGSENSE 0 6 DC 0
VSSENSE 0 7 DC 0
VBSENSE 0 8 DC 0
.OP
.TEMP -20 0 20 40 60
.DC VS 0  1 .1
.PRINT DC I(VDSENSE)
.ALTER
.PARAM LENG=50E-6
.END

*MTEST5B VDIODE VS. TEMPERATURE AND VSB TEST
*HSPICE SEMATECH MODEL QA NETLIST
*The object of this test is to check Vdiode (Vdb when Vdb=Vgb and Id=0.1uA*W/L)
*versus temperature and Vsb, for short and long devices.
.OPTION TNOM=27 GMIN=1E-14 NUMDGT=9 OPTS POST=2 NOPAGE
.WIDTH OUT=80
.INCLUDE 'nch.mod'
.PARAM LENG=0.5E-6
.PARAM WIDT=1.0E-6
M1 1 1 2 0 nch L=LENG W=WIDT
I1 0 1 DC 1E-7*WIDT/LENG
VS 2 0 DC 0
.OP
.DC VS 0 1 .1
.TEMP -20 0 20 40 60
.PRINT DC V(1)
.ALTER
.PARAM LENG=50E-6
.END

*MTEST6 ISAT*LMASK VS. LMASK TEST
*HSPICE SEMATECH MODEL QA NETLIST
*The object of this test is to check Isat*Lmask (where Isat=Id when Vdb=Vgb=Vdd
*and Lmask=masked channel length) versus Lmask.
.OPTION TNOM=27 GMIN=1E-14 NUMDGT=9 OPTS POST=2 NOPAGE
.WIDTH OUT=80
.INCLUDE 'nch.mod'
.PARAM LMASK=0.5E-6
M1 1 2 3 4 nch L=LMASK W=1.0E-6
VD 1 5 DC 5
VG 2 6 DC 5
VS 3 7 DC 0
VB 4 8 DC 0
VDSENSE 0 5 DC 0
VGSENSE 0 6 DC 0
VSSENSE 0 7 DC 0
VBSENSE 0 8 DC 0
.OP
```

```
.DC VB 0 0 1
.PRINT DC x=par('LMASK*I(VDSENSE)') y=par('LMASK')
.ALTER
.PARAM LMASK=1E-6
.ALTER
.PARAM LMASK=2E-6
.ALTER
.PARAM LMASK=4E-6
.ALTER
.PARAM LMASK=8E-6
.END

*MTEST6B VDIODE VS. LMASK TEST
*HSPICE SEMATECH MODEL QA NETLIST
*The object of this test is to check Vdiode (Vdb when Vdb=Vgb and Id=0.1uA*W/L)
*versus Lmask.
.OPTION TNOM=27 GMIN=1E-14 NUMDGT=9 OPTS POST=2 NOPAGE
.WIDTH OUT=80
.INCLUDE 'nch.mod'
.PARAM LMASK=0.5E-6
.PARAM WIDT=1.0E-6
VZ 2 0 DC 0
RZ 2 0 1
M1 1 1 0 0 nch L=LMASK W=WIDT
I1 0 1 DC 1E-7*WIDT/LENG
.OP
.DC VZ 0 0 1
.PRINT DC x=par('LMASK') V(1)
.ALTER
.PARAM LMASK=1E-6
.ALTER
.PARAM LMASK=2E-6
.ALTER
.PARAM LMASK=4E-6
.ALTER
.PARAM LMASK=8E-6
.END

*MTEST7 ISAT/WMASK VS. WMASK TEST
*HSPICE SEMATECH MODEL QA NETLIST
*The object of this test is to check Isat/Wmask (where Isat=Id when Vdb=Vgb=Vdd
*and Wmask=masked channel width) versus Wmask.
.OPTION TNOM=27 GMIN=1E-14 NUMDGT=9 OPTS POST=2 NOPAGE
.WIDTH OUT=80
.INCLUDE 'nch.mod'
.PARAM WMASK=0.5E-6
.PARAM LENG=1.0E-6
M1 1 2 3 4 nch L=LENG W=WMASK
VD 1 5 DC 5
VG 2 6 DC 5
VS 3 7 DC 0
VB 4 8 DC 0
VDSENSE 0 5 DC 0
VGSENSE 0 6 DC 0
VSSENSE 0 7 DC 0
VBSENSE 0 8 DC 0
.OP
.DC VB 0 0 1
.PRINT DC x=par('I(VDSENSE)/WMASK') y=par('WMASK')
.ALTER
.PARAM WMASK=1E-6
.ALTER
.PARAM WMASK=2E-6
.ALTER
```

```
.PARAM WMASK=4E-6
.ALTER
.PARAM WMASK=8E-6
.END

*MTEST7B VDIODE VS. WMASK TEST
*HSPICE SEMATECH MODEL QA NETLIST
*The object of this test is to check Vdiode (Vdb when Vdb=Vgb and Id=0.1uA*W/L)
*versus Wmask.
.OPTION TNOM=27 GMIN=1E-14 NUMDGT=9 OPTS POST=2 NOPAGE
.WIDTH OUT=80
.INCLUDE 'nch.mod'
.PARAM WMASK=0.5E-6
.PARAM LENG=1.0E-6
VZ 2 0 DC 0
RZ 2 0 1
M1 1 1 0 0 nch L=LENG W=WMASK
I1 0 1 DC 1E-7*WMASK/LENG
.OP
.DC VZ 0 0 1
.PRINT DC x=par('WMASK') V(1)
.ALTER
.PARAM WMASK=1E-6
.ALTER
.PARAM WMASK=2E-6
.ALTER
.PARAM WMASK=4E-6
.ALTER
.PARAM WMASK=8E-6
.END

*MTEST8 WEAK/MODERATE INVERSION TEST
*HSPICE SEMATECH MODEL QA NETLIST
*The object of this test is to check the transition from weak to moderate
*inversion in a given MOS model.
*For a Vds value in the saturation region, plot log(Id) vs. Vgs, including Vgs
*values well below threshold.
*There should be no discontinuities nor kinks.
.OPTION TNOM=27 GMIN=1E-14 NUMDGT=9 OPTS POST=2 NOPAGE
.WIDTH OUT=80
.INCLUDE 'nch.mod'
M1 1 2 3 4 nch
VD 1 5 DC 3
VG 2 6 DC 1
VS 3 7 DC 0
VB 4 8 DC 0
VDSENSE 0 5 DC 0
VGSENSE 0 6 DC 0
VSSENSE 0 7 DC 0
VBSENSE 0 8 DC 0
.OP
.DC VG 0 4 1E-3
.PRINT DC I(VDSENSE) x=par('log(I(VDSENSE))')
*         ID         log(ID)
.END

*MTEST9 GM/ID TEST
*HSPICE SEMATECH MODEL QA NETLIST
*The object of this test is to check the transconductance-to-current ratio
*gm/Id vs. Vgs, including Vgs values well below threshold, or vs. log(Id).
*There should be no discontinuities nor kinks.
.OPTION TNOM=27 GMIN=1E-14 NUMDGT=9 OPTS POST=2 NOPAGE
.WIDTH OUT=80
.INCLUDE 'nch.mod'
```

```
M1 1 2 3 4 nch
VD 1 5 DC 3
VG 2 6 DC 1
VS 3 7 DC 0
VB 4 8 DC 0
VDSENSE 0 5 DC 0
VGSENSE 0 6 DC 0
VSSENSE 0 7 DC 0
VBSENSE 0 8 DC 0
.OP
.DC VG 0 4 1E-3
.PRINT DC I(VDSENSE) x=par('log(I(VDSENSE))') y=par('lx7(M1)/I(VDSENSE)')
*         ID         log(ID)                   gm/ID
.END

*MTEST10 GDS TEST
*HSPICE SEMATECH MODEL QA NETLIST
*The object of this test is to observe the output conductance gds vs. Vds for
*one or more values of Vgs.
*There should be no discontinuities nor kinks.
.OPTION TNOM=27 GMIN=1E-14 NUMDGT=9 OPTS POST=2 NOPAGE
.WIDTH OUT=80
.INCLUDE 'nch.mod'
M1 1 2 3 4 nch
VD 1 5 DC 1
VG 2 6 DC 1
VS 3 7 DC 0
VB 4 8 DC 0
VDSENSE 0 5 DC 0
VGSENSE 0 6 DC 0
VSSENSE 0 7 DC 0
VBSENSE 0 8 DC 0
.OP
.DC VG 0 1 .1 VD 0 1 1E-3
.PRINT DC I(VDSENSE) lx8(M1)
*         ID         go
.END

*MTEST11 SERIES DEVICE FREQUENCY RESPONSE
*HSPICE SEMATECH MODEL QA NETLIST
*The object of this test is to check the frequency response of Id to a Vgs
*stimulus for a single very long-channel device and for an equivalent device
*made of two transistors in series (each having half the length of the single
*device, gates and bulks connected together, one drain connected to the other
*source).
*NOTE: This test should use device models with all parameters having to do with
*parasitics such as junction and overlap capacitances, series resistors, etc.
*removed, and with no source nor drain areas specified.
*The frequency responses should be identical.
.OPTION TNOM=27 GMIN=1E-14 NUMDGT=9 OPTS POST=2 NOPAGE
.WIDTH OUT=80
.INCLUDE 'nornch.mod'
m1 1 2 0 0 nornch w=3u l=100u
m2 3 2 4 0 nornch w=3u l=50u
m3 4 2 0 0 nornch w=3u l=50u
vd2 3 0 dc 4
vd 1 0 dc 4
vg 2 0 dc 3 ac 1
.ac dec 101 1 10g
.print ac im(vd) im(vd2)
.END

*MTEST12 RESISTIVE NOISE TEST
*HSPICE SEMATECH MODEL QA NETLIST
```

```
*The object of this test is to check the thermal noise of the MOS channel.
*Bias a device with a fixed Vgs in strong inversion, and at Vds=0 by placing a
*zero-value dc current source between drain and source.  Run a noise simulation
*for a frequency low enough so that the result is not affected by capacitances.
*The channel should show thermal noise voltage with power spectral density of
*4kTR where R=1/gds.
*k=Boltzmann's constant=1.3806226E-23  T=temperature in Kelvins='C+273.15
.OPTION TNOM=27 GMIN=1E-14 NUMDGT=9 OPTS POST=2 NOPAGE
.WIDTH OUT=80
.INCLUDE 'nornch.mod'
m1 1 2 0 3 nornch w=3u l=2u
id 0 1 dc 0
vb 3 0 dc 0
vin 2 0 dc 2 ac 1
.ac dec 10 1 1E9
.noise v(1) vin 1
.END

*MTEST13 NOISE WIDTH SCALING TEST (THIS NETLIST IS INCOMPLETE)
*HSPICE SEMATECH MODEL QA NETLIST
*The object of this test is to check the width scaling of 1/f noise.
*Bias a device in strong inversion saturation and run a noise simulation at
*frequencies where 1/f noise should be dominant.  Convert the noise current to a
*voltage across a one Ohm resistor (or, even better, a "noiseless resistor" via
*a self-dependent voltage-controlled current source).  Now, increase the channel
*width by a factor of 10 and see whether the noise power spectral density
*decreases by a factor of 10.  Also, see if the noise current is insensitive to
*changes in Vgs, as it should be for most devices.
.OPTION TNOM=27 GMIN=1E-14 NUMDGT=9 OPTS POST=2 NOPAGE
.WIDTH OUT=80
.INCLUDE 'nch.mod'
.PARAM WIDT=1.0E-6
M1 1 2 3 4 nch W=WIDT L=1.0E-6
VD 1 5 DC 5
VG 2 6 DC 3 AC 1
VS 3 7 DC 0
VB 4 8 DC 0
VDSENSE 0 5 DC 0
VGSENSE 0 6 DC 0
VSSENSE 0 7 DC 0
VBSENSE 0 8 DC 0
.OP
.ALTER
.PARAM WIDT=1.0E-5
.END

*MTEST14 TRANSCONDUCTANCE VS. VGB TEST
*HSPICE SEMATECH MODEL QA NETLIST
*The object of this test is to check transconductance versus a fine Vgb sweep.
.OPTION TNOM=27 GMIN=1E-14 NUMDGT=9 OPTS POST=2 NOPAGE
.WIDTH OUT=80
.INCLUDE 'nch.mod'
M1 1 2 3 4 nch
VD 1 5 DC 1
VG 2 6 DC 1
VS 3 7 DC 0
VB 4 8 DC 0
VDSENSE 0 5 DC 0
VGSENSE 0 6 DC 0
VSSENSE 0 7 DC 0
VBSENSE 0 8 DC 0
.OP
.DC VG 0 4 2E-3
.PRINT DC lx7(M1)
```

```
*          gm
.END

*MTEST15 OUTPUT CONDUCTANCE WIDE RANGE TEST
*HSPICE SEMATECH MODEL QA NETLIST
*The object of this test is to check output conductance over a wide bias range
*with a fine Vdb step.
.OPTION TNOM=27 GMIN=1E-14 NUMDGT=9 OPTS POST=2 NOPAGE
.WIDTH OUT=80
.INCLUDE 'nch.mod'
M1 1 2 3 4 nch
VD 1 5 DC 1
VG 2 6 DC 1
VS 3 7 DC 0
VB 4 8 DC 0
VDSENSE 0 5 DC 0
VGSENSE 0 6 DC 0
VSSENSE 0 7 DC 0
VBSENSE 0 8 DC 0
.OP
.DC VD 0 1 1E-3 VG -2 5 .1
.PRINT DC lx8(M1)
*          go
.END

*MTEST16 OUTPUT CONDUCTANCE LIMITED RANGE TEST
*HSPICE SEMATECH MODEL QA NETLIST
*The object of this test is to check output conductance with fixed Vgb and Vsb
*values over a limited range of Vdb with a fine Vdb sweep.
.OPTION TNOM=27 GMIN=1E-14 NUMDGT=9 OPTS POST=2 NOPAGE
.WIDTH OUT=80
.INCLUDE 'nch.mod'
M1 1 2 3 4 nch
VD 1 5 DC 1
VG 2 6 DC 1
VS 3 7 DC 0
VB 4 8 DC 0
VDSENSE 0 5 DC 0
VGSENSE 0 6 DC 0
VSSENSE 0 7 DC 0
VBSENSE 0 8 DC 0
.OP
.DC VD 0 1 1E-3 VG 0 1 .1
.PRINT DC lx8(M1)
*          go
.END

*MTEST17 DRAIN CURRENT SYMMETRY TEST
*HSPICE SEMATECH MODEL QA NETLIST
*The object of this test is to check the symmetry of Id.
*Drive a MOSFET with Vgb, Vsb=Vsb-Vx, and Vdb=Vdb+Vx.
*Id must be an odd function of Vx, so Id(Vx)=-Id(-Vx), and the second partial
*derivative of Id with respect to Vx must be zero at Vx=0.
*Plot gx=partial derivative of Id with respect to Vx for a fine grid near Vx=0V.
*Asymmetric models will have a break in gx near Vx=0.
.OPTION TNOM=27 GMIN=1E-14 NUMDGT=9 OPTS POST=2 NOPAGE
.WIDTH OUT=80
.INCLUDE 'nch.mod'
VX 7 0 DC 0
RX 7 0 1
M1 1 2 3 0 nch
VGB 2 0 DC 3
VDB1 1 5 DC 2
VSB1 3 6 DC 1
```

```
E1 0 6 7 0 1
E2 5 0 7 0 1
.OP
.DC VX -.1 .1 .001
.PRINT DC I1(M1)
.END

*MTEST18 SLOPE RATIO TEST
*HSPICE SEMATECH MODEL QA NETLIST
*The object of this test is to check the asymptotic Vdb behavior.
*Consider I1(Vdb=V1) and I2(Vdb=V2) for small Vdb and Vsb=0.
*Plot SR=((I2+I1)*(V2-V1)/((I2-I1)*(V2+V1)) against Vgb.  This is the ratio of
*the slope of the line through the origin and the midpoint of (V1,I1) and
*(V2,I2) to the slope of the line through (V1,I1) and (V2,I2).  In subthreshold,
*SR should reach an asymptote determined by T and by the values of V1 and V2.
*Above threshold, SR should approach unity (1.0).  This shows problems with
*kinks/glitches and with poor subthreshold modeling.
.OPTION TNOM=27 GMIN=1E-14 NUMDGT=9 OPTS POST=2 NOPAGE
.WIDTH OUT=80
.INCLUDE 'nch.mod'
.PARAM GATE=0
.PARAM VDRAIN1=0.1
.PARAM VDRAIN2=0.2
M1 1 3 0 0 nch
M2 4 6 0 0 nch
VD1 1 2 DC VDRAIN1
VSNS1 2 0 DC 0
VG1 3 0 DC GATE
VD2 4 5 DC VDRAIN2
VSNS2 5 0 DC 0
VG2 6 0 DC GATE
.DC GATE 0 2 .001
.PRINT DC
+ x=par('((I(VSNS2)+I(VSNS1))*(V(4)-V(1)))/((I(VSNS2)-I(VSNS1))*(V(4)+V(1)))')
.END

*MTEST19 TREETOP CURVE TEST
*HSPICE SEMATECH MODEL QA NETLIST
*The object of this test is to check asymptotic Vgb behavior in subthreshold.
*For a long channel MOSFET with uniform doping, gm/Id in subthreshold
*asymptotically approaches a value that depends on Vgb. For large Vgb, the
*asymptote approaches the reciprocal thermal voltage. The asymptotic behavior
*is in the absence of junction leakage currents. The behavior is observed in
*practice in long channel MOSFETs. The asymptotic value is nearly, but not
*quite, reached for short MOSFETs. This shows problems in models with simple
*(unphysical) subthreshold modeling.
.OPTION TNOM=27 GMIN=1E-14 NUMDGT=9 OPTS POST=2 NOPAGE
.WIDTH OUT=80
.INCLUDE 'nch.mod'
M1 1 2 0 0 nch L=100E-6 W=10E-6
VD 1 3 DC 2
VG 2 0 DC 1
VDSENSE 0 3 DC 0
.OP
.DC VG 0 5 .01
.PRINT DC y=par('lx7(M1)/I(VDSENSE)')
*                 gm/Id
.END

*MTEST20 GATE CAPACITANCE TEST
*HSPICE SEMATECH MODEL QA NETLIST
*The object of this test is to check gate capacitance terms over bias.
*Plot Cgg, Cgb, and Cgs+Cgd against Vgb for Vsb=0 and Vdb=0 (and Vdb=1.5V),
*using a fine Vgb step.
```

```
*This shows unphysical abrupt boundaries at flatband and threshold.
.OPTION TNOM=27 GMIN=1E-14 NUMDGT=9 OPTS POST=2 NOPAGE
.WIDTH OUT=80
.INCLUDE 'nch.mod'
M1 1 2 3 4 nch
VD 1 5 DC 0
VG 2 6 DC 1
VS 3 7 DC 0
VB 4 8 DC 0
VDSENSE 0 5 DC 0
VGSENSE 0 6 DC 0
VSSENSE 0 7 DC 0
VBSENSE 0 8 DC 0
.OP
.DC VG -5 5 .01
.OPTION DCCAP
.PRINT DC lx18(M1) x=par('lx20(M1)+lx19(M1)')
*         Cgg        Cgs+Cgd
+y=par('lx18(M1)-lx19(M1)-lx20(M1)')
*  Cgb=Cgg-Cgd-Cgs
.ALTER
VD 1 5 DC 1.5
.END

*MTEST21 CAPACITANCE COEFFICIENT TEST
*HSPICE SEMATECH MODEL QA NETLIST
*The object of this test is to check capacitance terms over bias.
*Plot Cgs, Cgd, Cgb, Cbs, Cbd, Csd, Cdg, Cdb, Cbg against Vdb for Vsb=0 and
*Vgb=Vdd.  This shows asymmetries and discontinuities, and inconsistent
*saturation, wrong sign.
.OPTION TNOM=27 GMIN=1E-14 NUMDGT=9 OPTS POST=2 NOPAGE
.WIDTH OUT=80
.INCLUDE 'nch.mod'
M1 1 2 3 4 nch
VD 1 5 DC 5
VG 2 6 DC 5
VS 3 7 DC 0
VB 4 8 DC 0
VDSENSE 0 5 DC 0
VGSENSE 0 6 DC 0
VSSENSE 0 7 DC 0
VBSENSE 0 8 DC 0
.OP
.OPTION DCCAP
.DC VD -5 5 .01
.PRINT DC lx20(M1) lx19(M1) a=par('lx18(M1)-lx19(M1)-lx20(M1)')
*         Cgs      Cgd        Cgb=Cgg-Cgd-Cgs
.PRINT DC lx23(M1) lx22(M1) b=par('lx33(M1)-lx19(M1)-lx22(M1)')
*         Cbs      Cbd        Csd=Cdd-Cgd-Cbd
.PRINT DC lx32(M1) lx21(M1) c=par('lx33(M1)-lx32(M1)-lx34(M1)')
*         Cdg      Cbg        Cdb=Cdd-Cdg-Cds
.END

*MTEST22 OUTPUT CONDUCTANCE TEST
*HSPICE SEMATECH MODEL QA NETLIST
*The object of this test is to check output conductance on a log scale.
*Plot log(gds) versus Id. This shows bugs in output conductance modeling and
*kinks/glitches at region boundaries.
.OPTION TNOM=27 GMIN=1E-14 NUMDGT=9 OPTS POST=2 NOPAGE
.WIDTH OUT=80
.INCLUDE 'nch.mod'
M1 1 2 3 4 nch
VD 1 5 DC 1
VG 2 6 DC 1
```

```
VS 3 7 DC 0
VB 4 8 DC 0
VDSENSE 0 5 DC 0
VGSENSE 0 6 DC 0
VSSENSE 0 7 DC 0
VBSENSE 0 8 DC 0
.OP
.DC VD 0 1 1E-3 VG 0 1 .1
.PRINT DC I(VDSENSE) x=par('log(lx8(M1))/log(10)')
*         ID         logbase10(go)
.END
```

simple batch script:

```
./hspice mtest2.sp > mtest2.lis
./hspice mtest3.sp > mtest3.lis
./hspice mtest4.sp > mtest4.lis
./hspice mtest5.sp > mtest5.lis
./hspice mtest5b.sp > mtest5b.lis
./hspice mtest6.sp > mtest6.lis
./hspice mtest6b.sp > mtest6b.lis
./hspice mtest7.sp > mtest7.lis
./hspice mtest7b.sp > mtest7b.lis
./hspice mtest8.sp > mtest8.lis
./hspice mtest9.sp > mtest9.lis
./hspice mtest10.sp > mtest10.lis
./hspice mtest11.sp > mtest11.lis
./hspice mtest12.sp > mtest12.lis
./hspice mtest13.sp > mtest13.lis
./hspice mtest14.sp > mtest14.lis
./hspice mtest15.sp > mtest15.lis
./hspice mtest16.sp > mtest16.lis
./hspice mtest17.sp > mtest17.lis
./hspice mtest18.sp > mtest18.lis
./hspice mtest19.sp > mtest19.lis
./hspice mtest20.sp > mtest20.lis
./hspice mtest21.sp > mtest21.lis
./hspice mtest22.sp > mtest22.lis
```

nch.mod:

```
.model nch nmos level=28 muz=600 x3ms=5 vfb0=-0.3 k1=0.6 phi0=0.65 cj=3e-4
+ cjsw=3e-10 js=1e-5 rsh=0 acm=2 ld=0.05u cgdo=2e-10 cgso=2e-10 tox=200
*note this is an arbitrary model, a complete typical model should be used.
```

nornch.mod:

```
.model nornch nmos level=28 muz=600 x3ms=5 vfb0=-0.3 k1=0.6 phi0=0.65 cj=3e-4
+ cjsw=3e-10 js=1e-5 rsh=0 acm=2 ld=0.05u cgdo=2e-10 cgso=2e-10 tox=200
*note this is an arbitrary model, a typical model (with parasitic resistances
*turned off) should be used.
```