

***DISEÑO Y FABRICACIÓN DE UN RECEPTOR
DIDÁCTICO COMERCIAL DE FM
CON RDS (RADIO DATA SYSTEM) .***

Realizado por: Elyoussoufi, Ilyass.

***Tutores: Roldán Aranda, Andrés.
Jiménez Molinos, Francisco.***

***FACULTAD DE CIENCIAS.
UNIVERSIDAD DE GRANADA.***

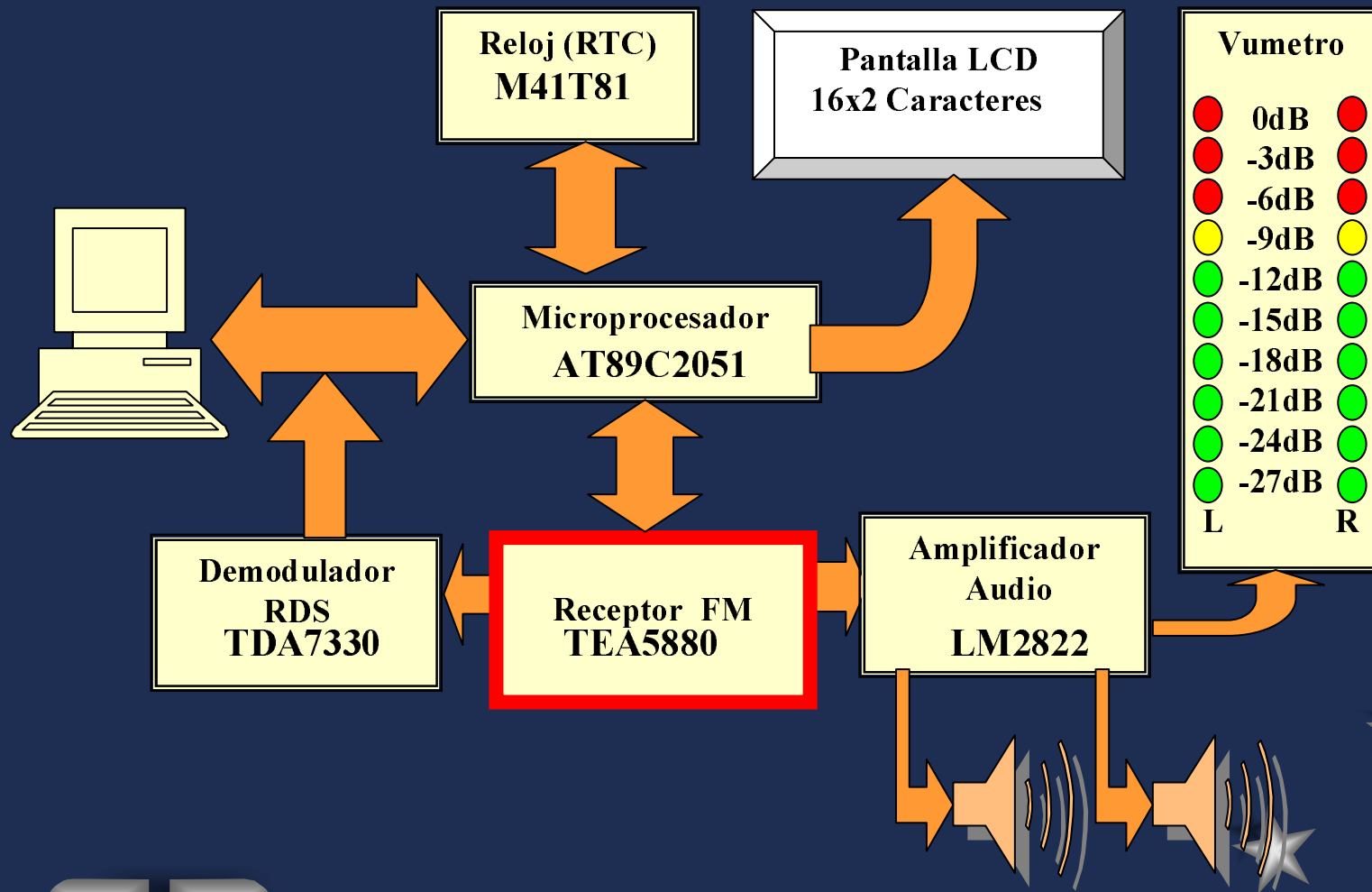


Requisitos del proyecto

- Receptor FM comercial
- Decodificador RDS
- Reloj de tiempo real
- Control mediante Microcontrolador
- Interfaz con el LCD
- Interfaz con ordenador
- Caja de metacrilato



Diagrama de bloques del proyecto



Espectro de la señal FM múltiplex (FMMPX) con RDS

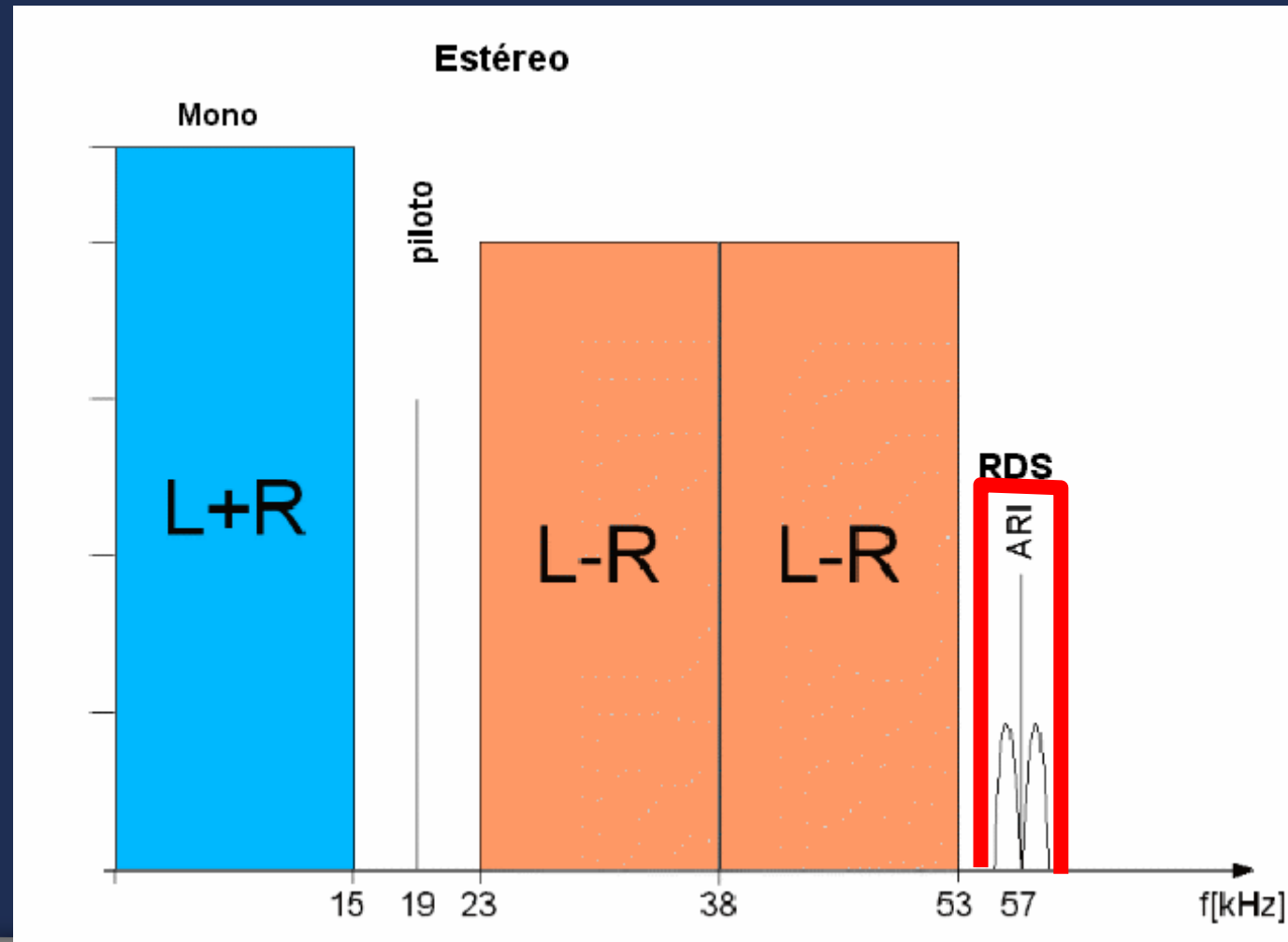
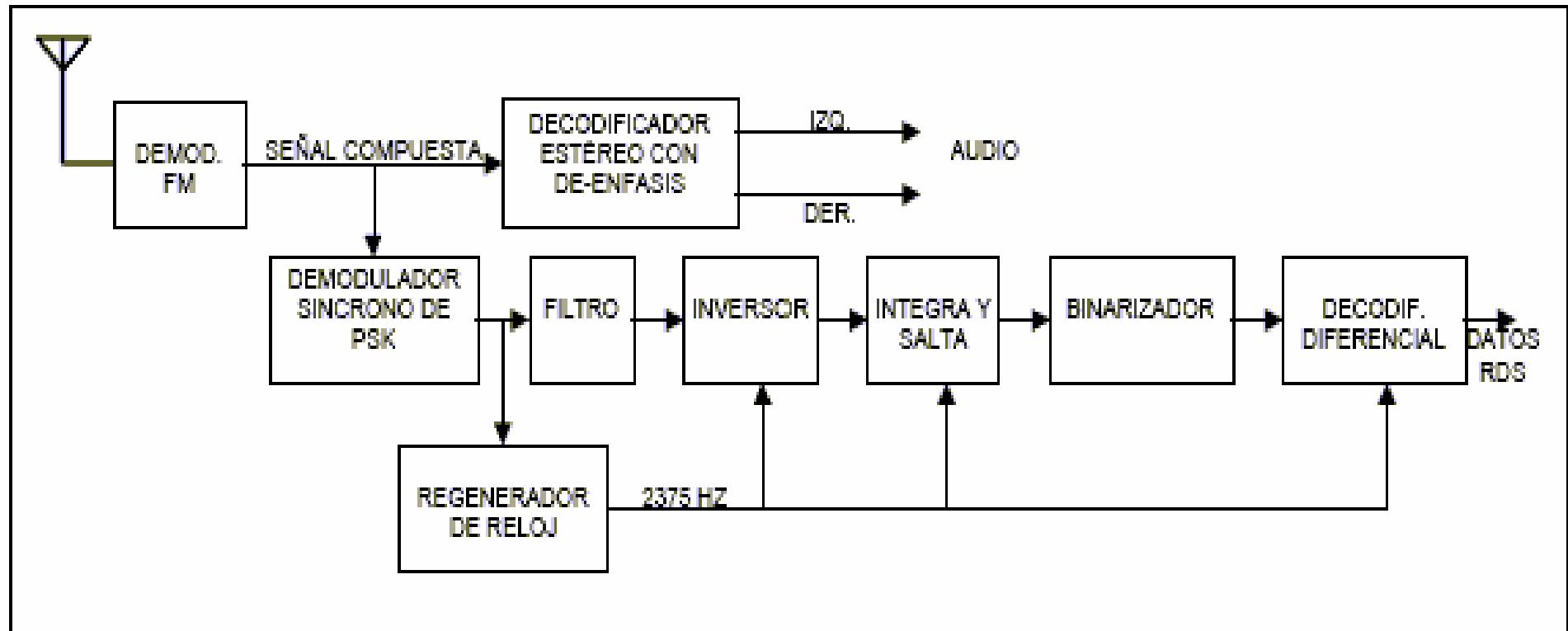


Diagrama de bloques del demodulador RDS



Paquete de información en el sistema RDS

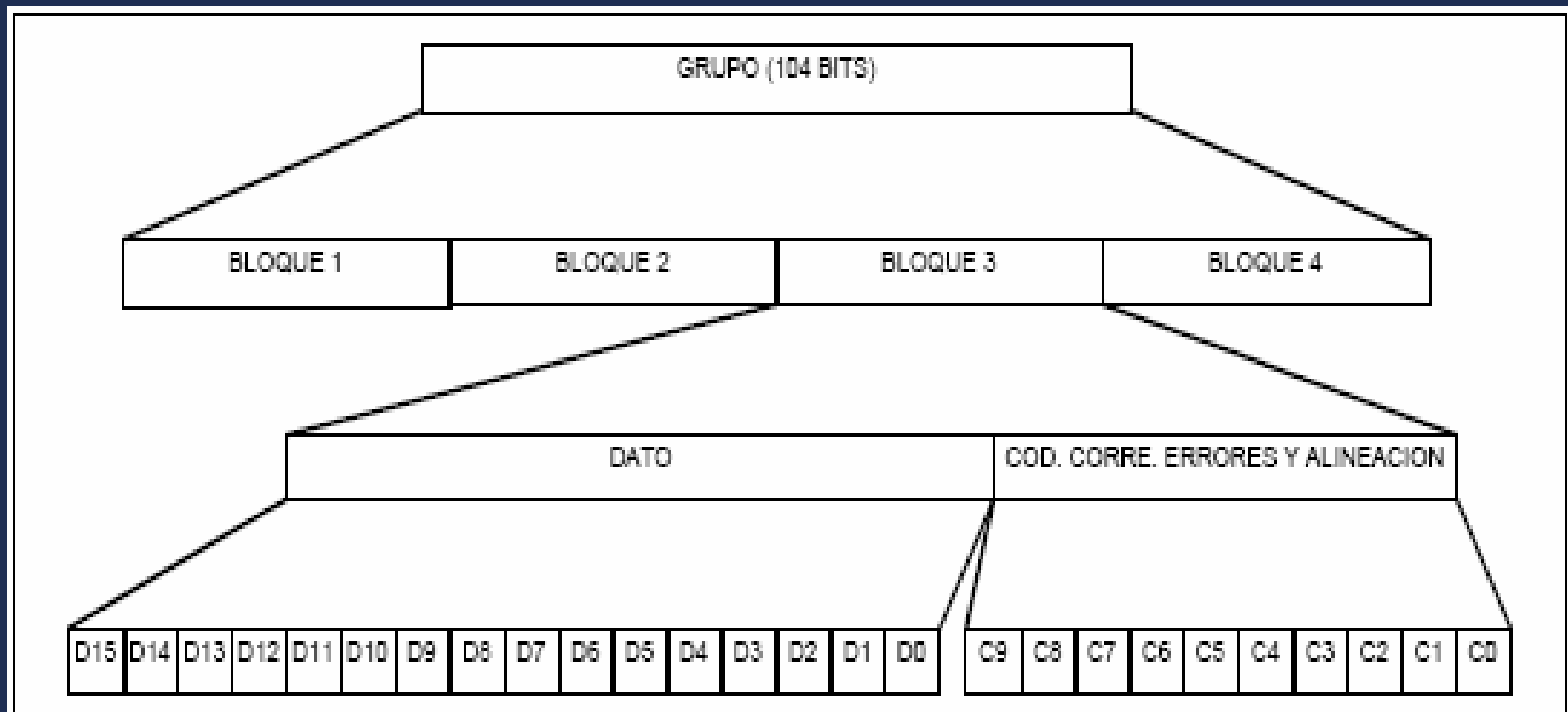
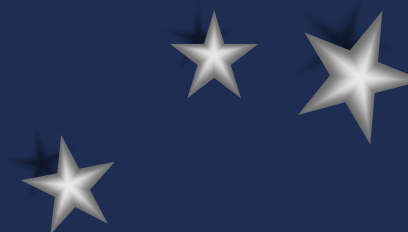
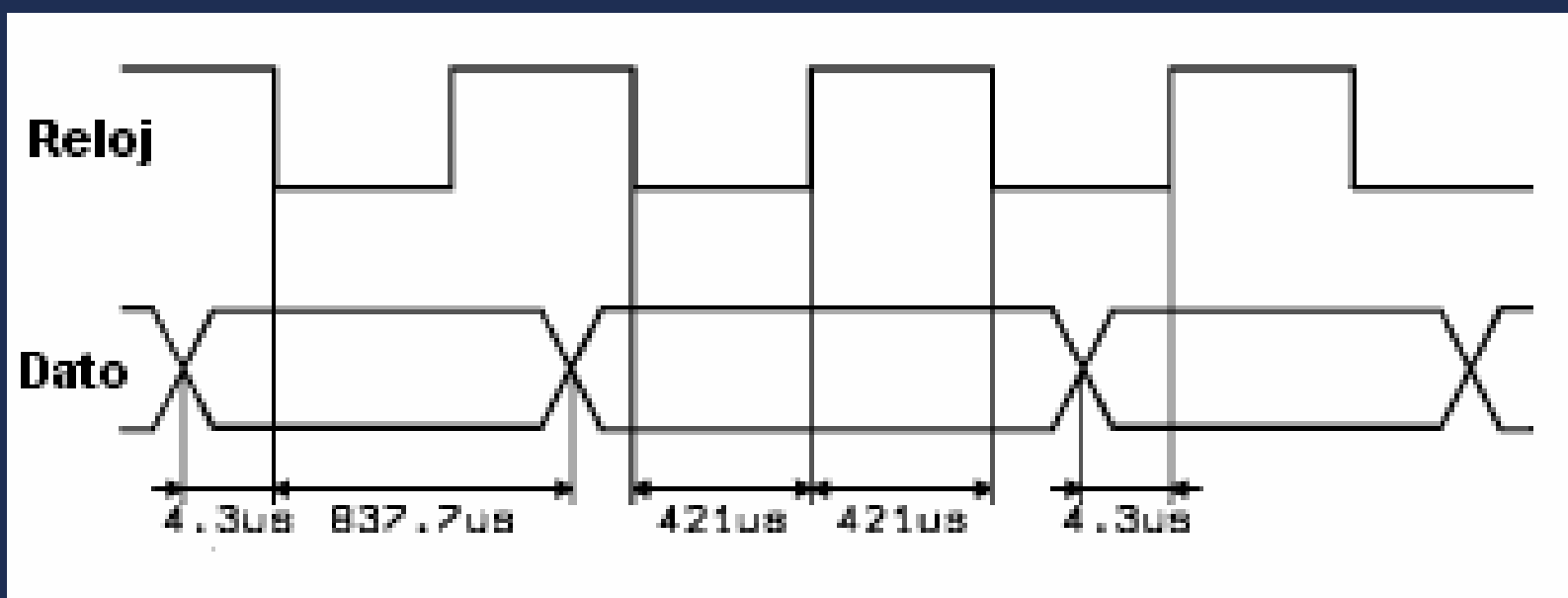


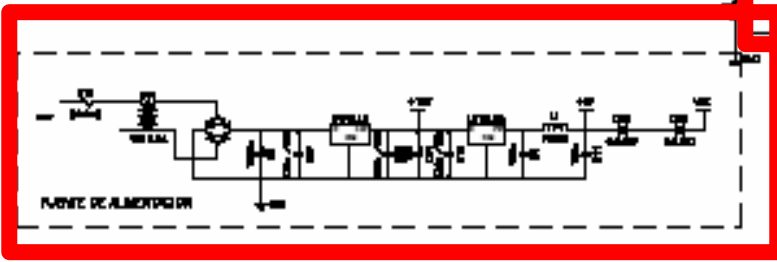
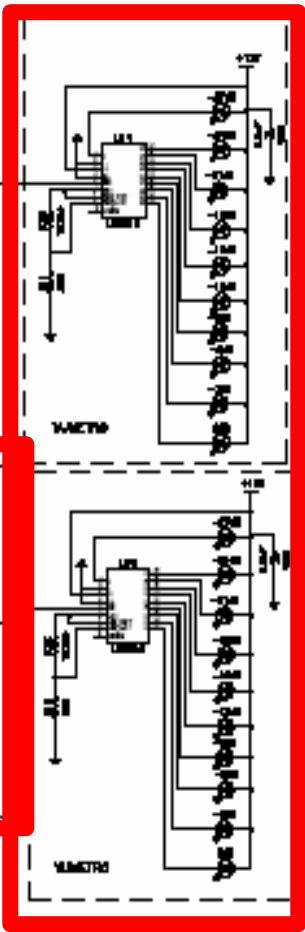
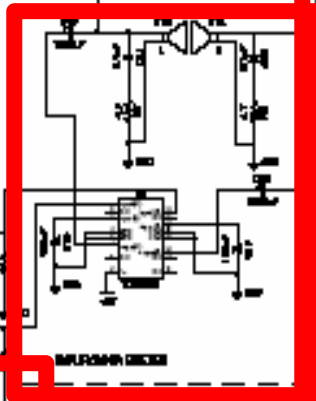
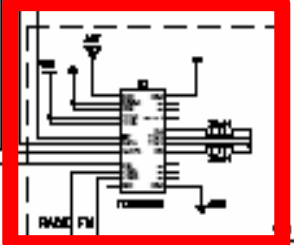
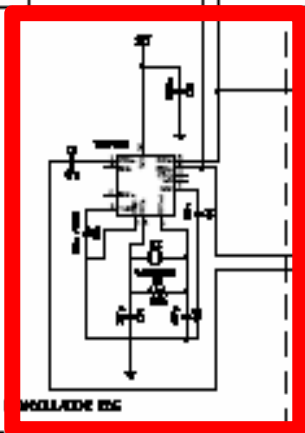
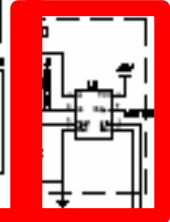
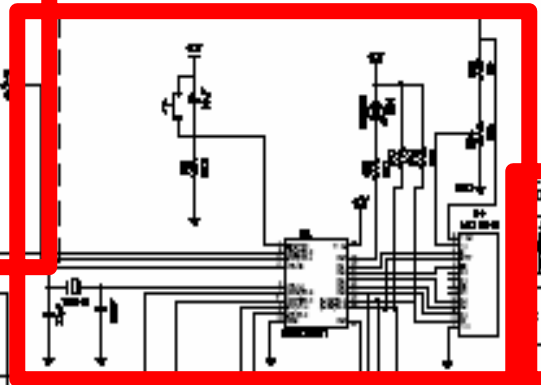
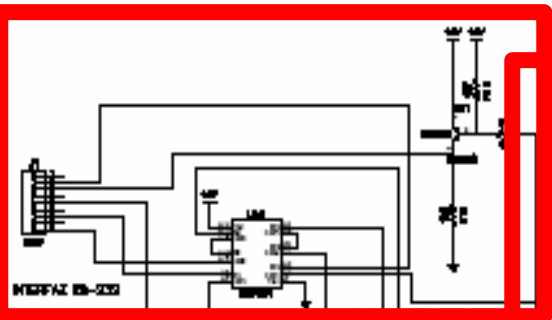
Diagrama de tiempo de la señal RDS



Ejemplo de aplicaciones de la señal RDS

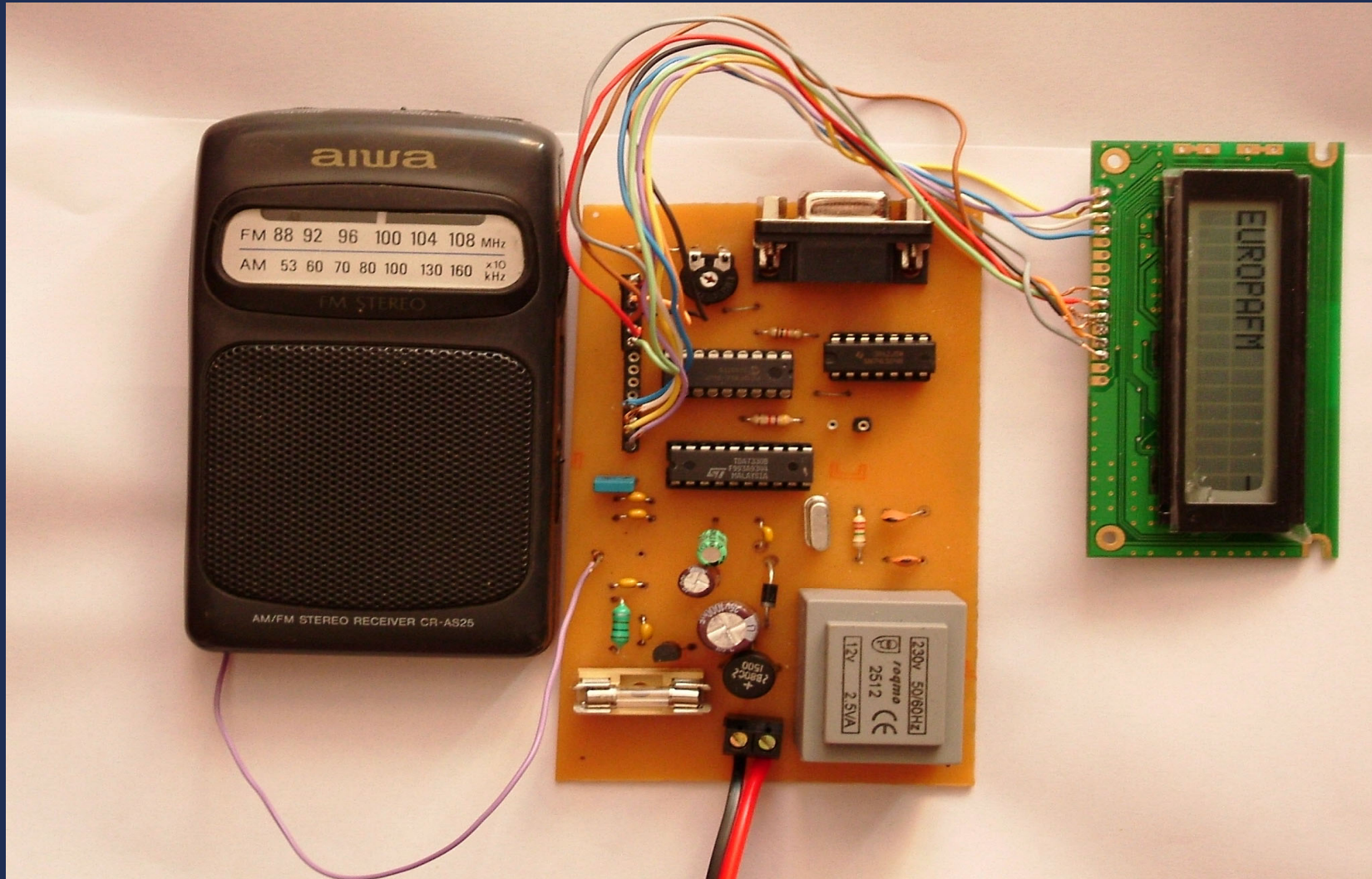
- Nombre del programa
- Tipo de programa
- Radio texto
- Anuncios de trafico
- “Radio paging”
- Otras aplicaciones: dGPS, TMC



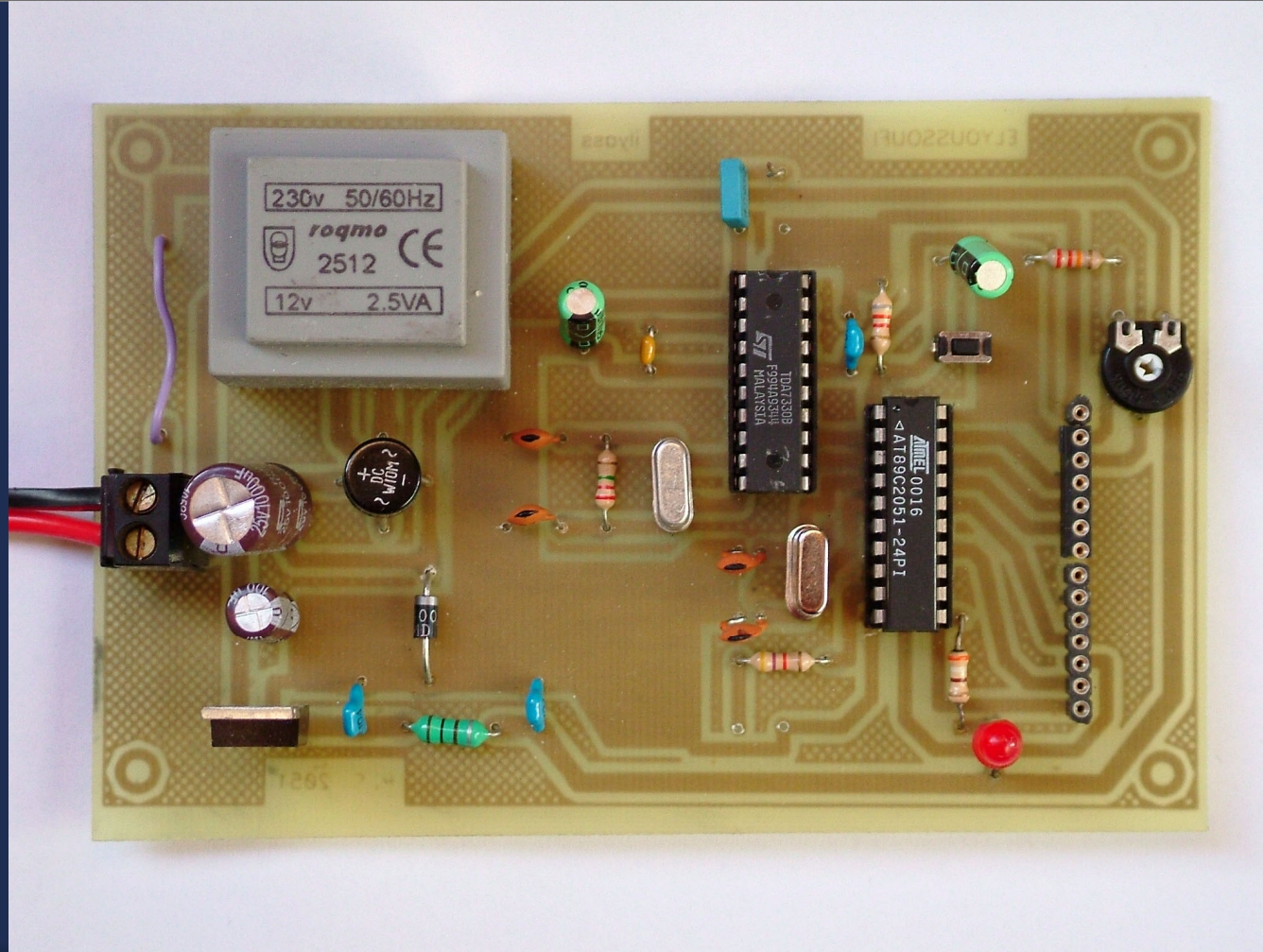


Título: Prototipo Final			
Clase:	Proyecto	4	Rev:
Auto:	1-10-2000	Diseno por:	Diseno Final
Plano en:	Prototipo Final	Sheet:	1 of 1

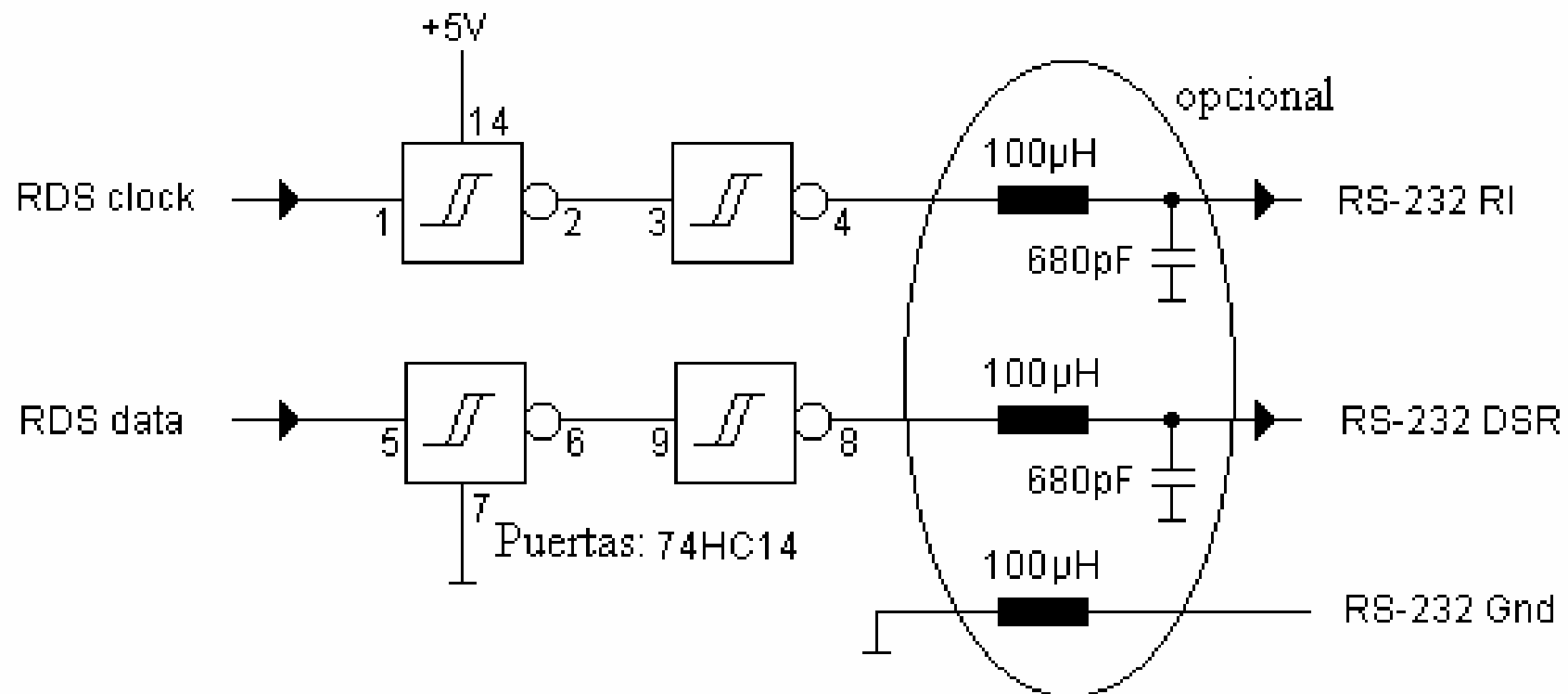
Prototipo 1: Interfaz RDS con el LCD a través del 16F84



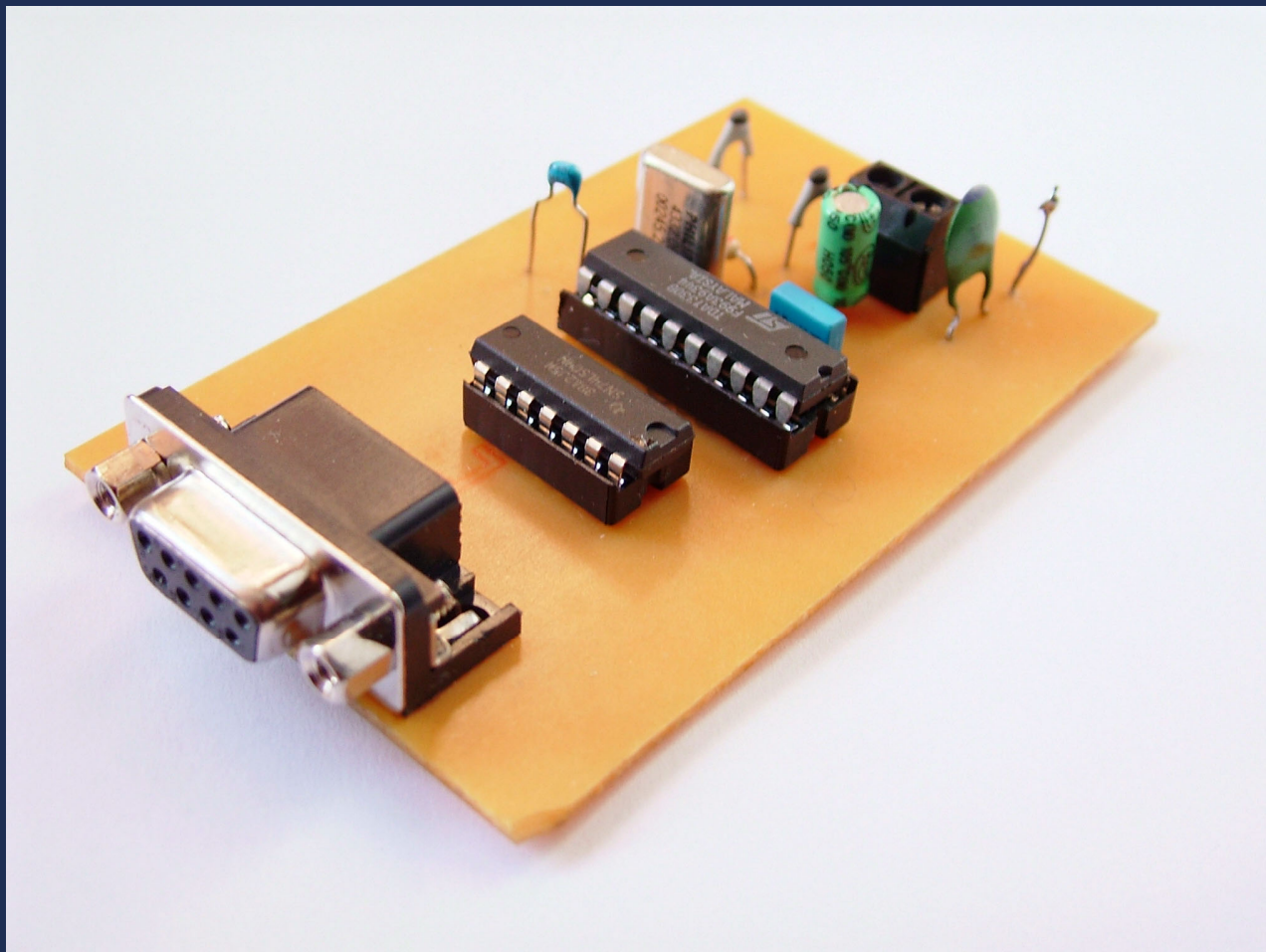
Prototipo 2: interfaz RDS con el LCD a través del 89C2051



Esquema del conexionado hardware



Prototipo 3: Interfaz RDS con el Ordenador



Software interfaz con ordenador

RDS Decoder 3.0

File BDS System 2

Signal Quality

Status: Signal BER
SYNC Avg 61%
Groups / faulty: 80 / 27

Bit Error Rate

Block correction
Correction failure

Regional Information / Decoder Information

Country: [Germany, ...] Coverage: Supra-regional DI value: 1 Interpretation: Stereo

Service

PS: SWR3
PI: D3A3
ECC: []
Service Details: LA TP TA MS
PTy (s): Pop Music

Date and Time

Date: [] Time: [] UTC: []

EON

Data Switch

Radio Text

A: SWR3 HILINE zum Lesen * Radiotext * SWWVWRRRRRDRREII *
B: []

Group Detector

0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
A: [] [] [] [] [] [] [] [] [] [] [] [] [] [] []
B: [] [] [] [] [] [] [] [] [] [] [] [] [] [] []

Radio Paging Viewer (Basic Paging Protocol)

Group codes in this network: 40..69

Type	Date / Time	Address	Message
[]	11/12 12:46:40	400040	C1123133,110,J8482,1,C03263600,JH0401MIG%844-%842-%836-%834-%832-%830-%828-%826
[]	11/12 12:46:43	400490	C1111071,100,J8481,1,C0326337777401 +S1+H1722+H1752+ JH0116L03/10H0201JOLOCHE
[]	11/12 12:46:58	404713	ALARME
[]	11/12 12:47:48	400490	C1111071,100,J8481,3,SJH0210M17H47JH0216LHH:MM
[]	11/12 12:47:51	400490	C1111071,110,J8480,0,C03263300,JH0401MIG%812-%814-%816-%818-%820-%822-%824-%826
[]	11/12 12:48:07	404713	ALARME

Group Viewer

Select groups

Group	%	Cnt A	Cnt B	Cnt C	Cnt D
[] 0A (Tune/Sw)	32.6	D3A3	0549	6D75	5357
[] 0B (Tune/Sw)	8.5	F203	1010	0000	0000
[] 1A (PIN/SLC)					

Select All Select None Reset Indicators

Group contents: 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15

Group	Blk 1	Blk 2	Blk 3	Blk 4
2A	D3A3	2544	%D	4C65 Le 7365 se
0A	D3A3	0549	I	6D75 mu 5357 Sw
11A	D3A3	8544	ID	FE46 F 2001
6A	D3A3	654A	eJ	0123 # 4567 Eg
2A	D3A3	2545	%E	6E20 n 2A20 *
14A	D3A3	E542	YB	5232 R2 D5A2 i

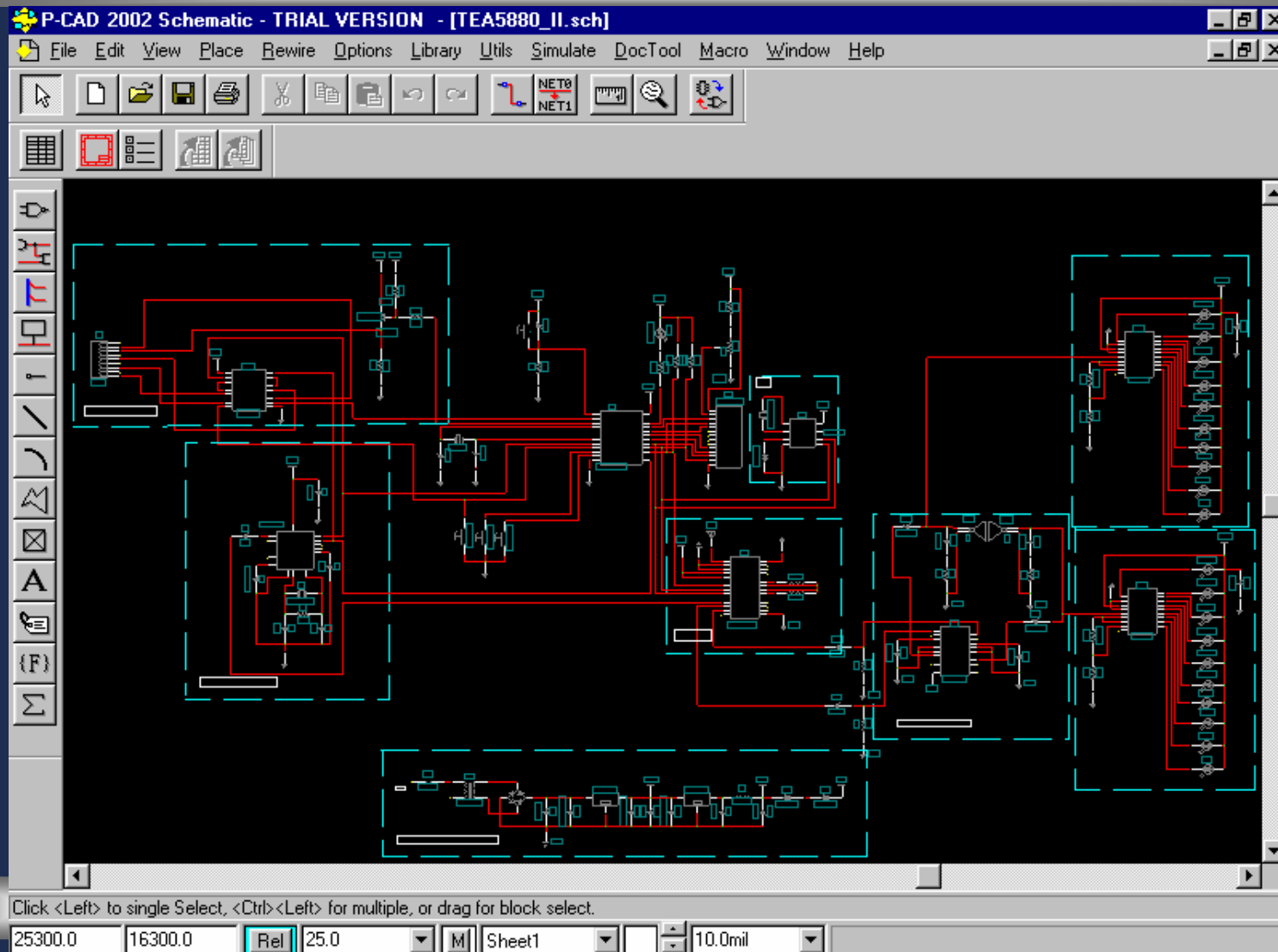
Clear list Write binary protocol file Write ASCII protocol file File options...

Approximate group timing

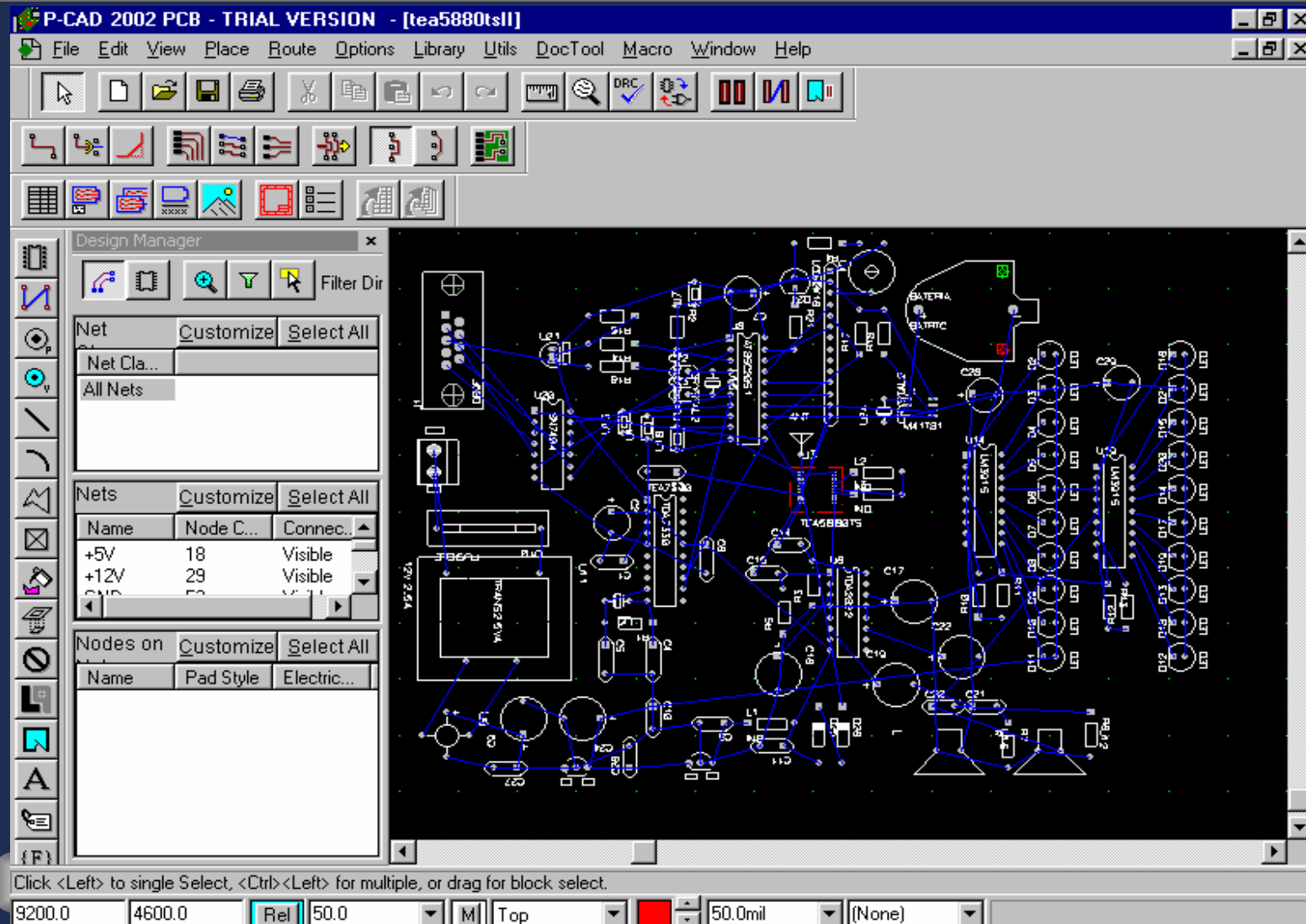
Time	Group type
0:03:01	0A
0:03:01	11A
0:03:01	6A
0:03:01	2A
0:03:01	14A

Clear list Display system time Display stop watch time Reset stop watch

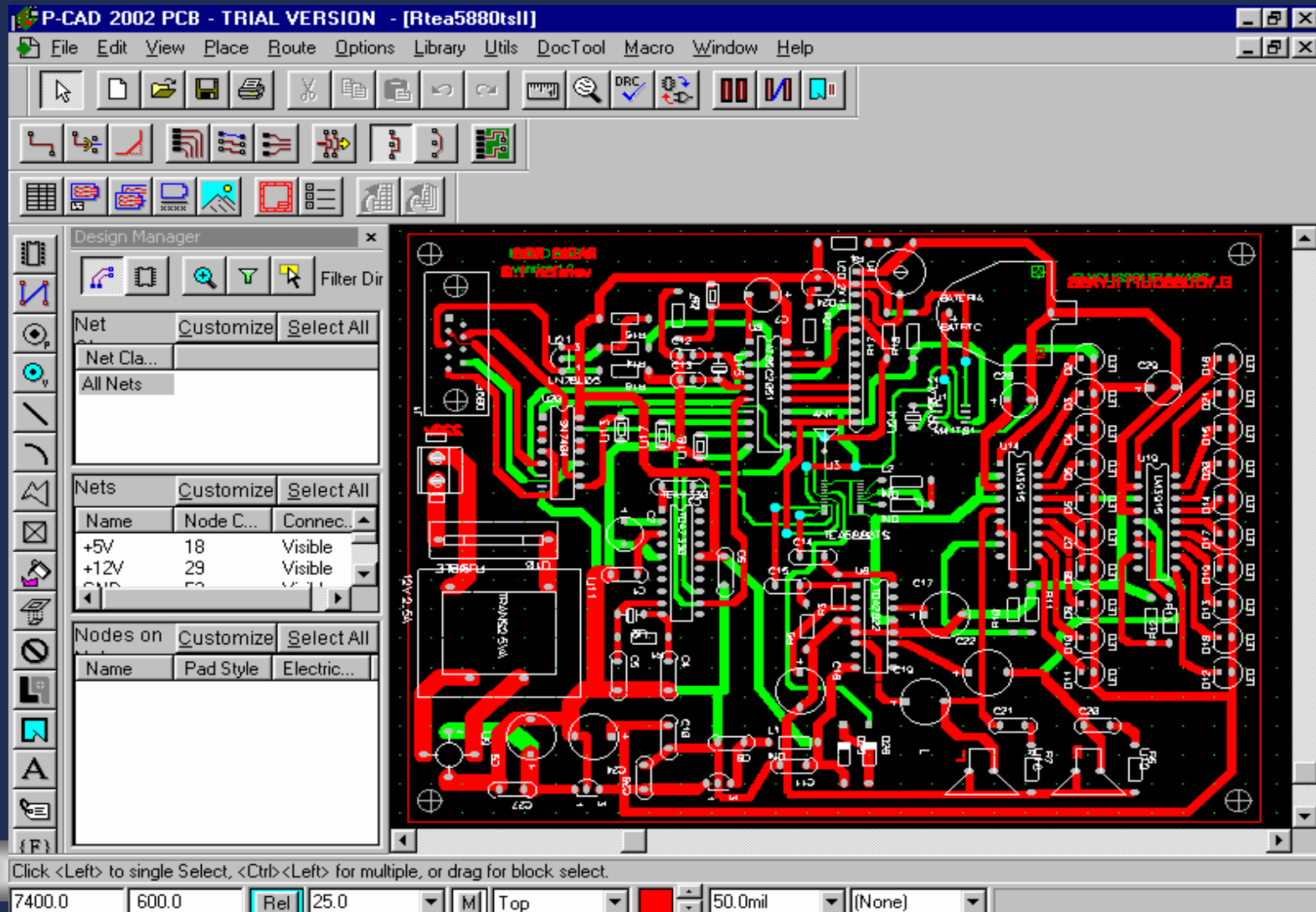
Radio RDS en P-CAD SCH



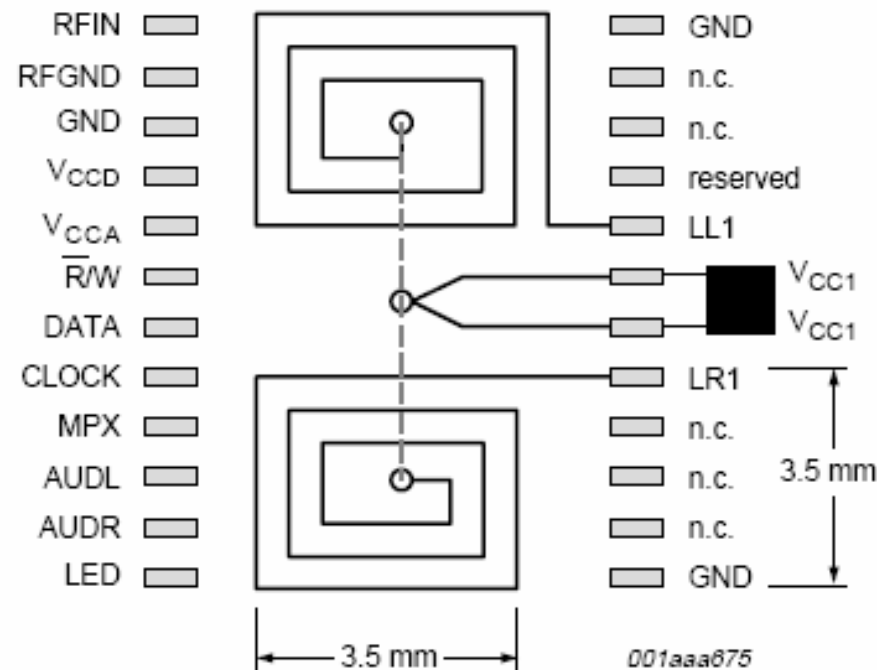
Colocación de los componentes del circuito



Diseño final de la placa de circuito impreso de la radio RDS



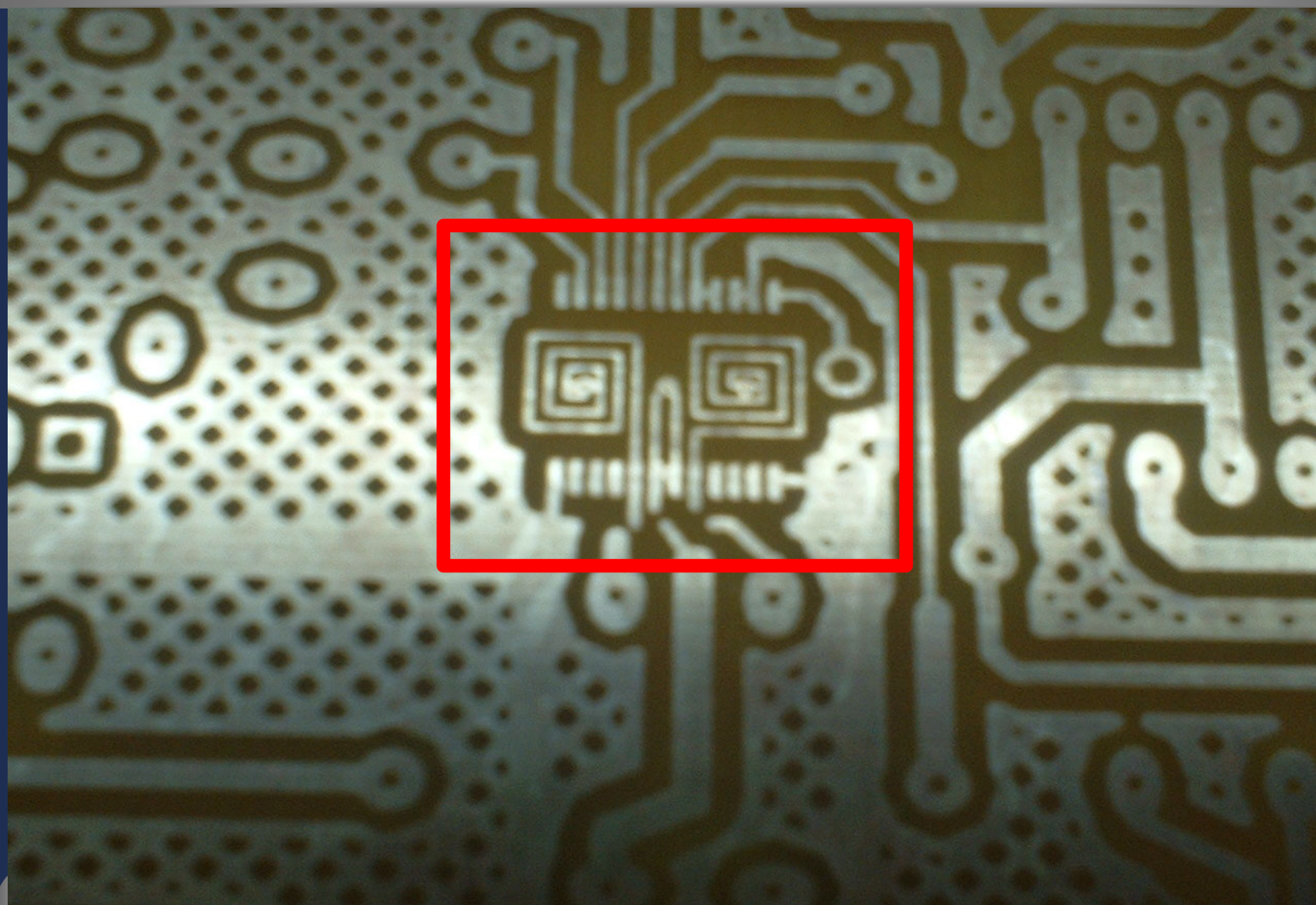
Dimensión de las bobinas que necesita la radio



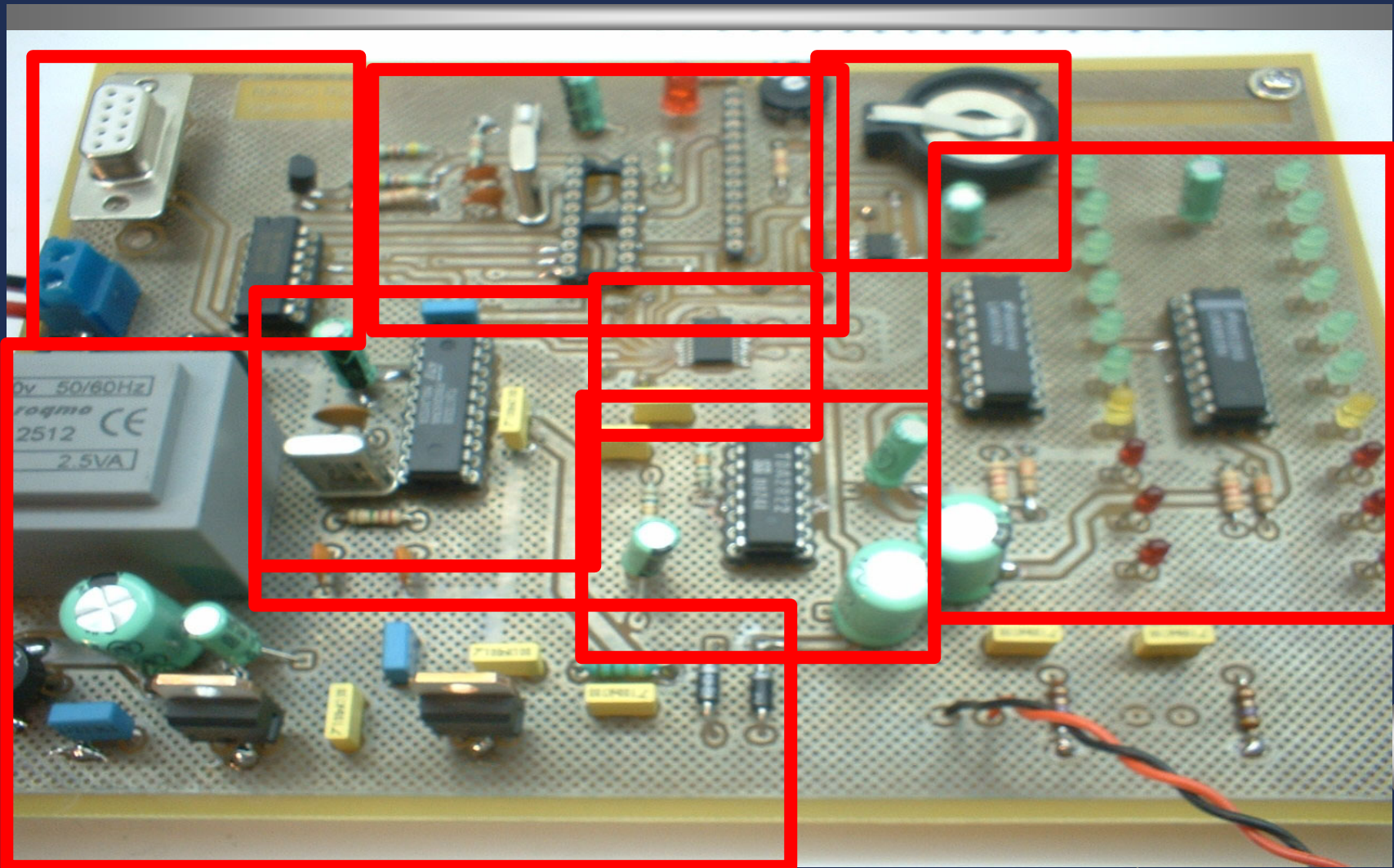
- (1) Width of printed-circuit board trace = 0.15 mm; spacing between printed-circuit board trace = 0.15 mm.
- (2) Pins 14, 15, 16, 21, 22 and 23 are not connected.

Fig 10. Printed-circuit board layout.

Prototipo final, cara de pistas



Prototipo final, cara de componentes



Resumen:

- Investigación
- Documentación
- Elección de componentes
- Desarrollo del hardware
- Desarrollo del software



Mejoras futuras

- Reducir el tamaño
- Reducir el coste
- Control del receptor desde el PC

