Assessment Of Blind Via Holes – An Alternative Approach

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While the use of blind vias has become fairly common in electronics manufacturing today, inspection of via holes during fabrication is still problematic. We take a look at a simple and easy way of assessing blind vias that makes failure analysis easier to perform and produces less controversy.

It has become common practice to use blind vias in many portable electronics products. Experience has shown that this method of interconnection is reliable provided the fabrication process is well defined and controlled. Both through hole, blind and buried vias can stand-up to conventional and now Lead-free manufacture as the length of the barrel is fairly short. It is, however, still difficult to inspect via locations during the fabrication process and there is often great debate on the cause of any failure or if a particular via is satisfactory of not. The images in Figure 1 show typical examples of different via connections.

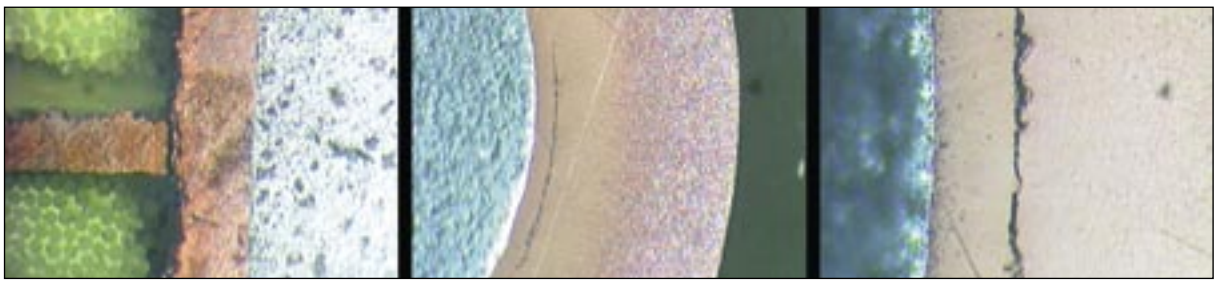
It was a little unfortunate that the IPC-A-600G did not address the issue of via assessment when it was last updated and released during 2004. It is hoped that this will be addressed during any future planed revisions. Blind and buried vias have been used in the industry for many years. Great experience exists, but very few standards or inspection guidelines exist for a company to reference. Producing a microsection is still the most common method of via assessment. Engineers who have learned the procedures of microsectioning will state that it requires great level of skill and experience to correctly prepare and make assessment of a blind via. Often the assessment can be debated due to the methods of sectioning and the final etching process used on the Copper layers.

Interconnection Stress Test

Recently Interconnection Stress Test (IST) has been used by companies as an assessment tool to examine the reliability under simulated operational conditions. A test coupon is designed to simulate the via pattern based on the design rules used on a product family. The test coupon features a heating circuit which allows a DC current to pass through internal layers to simulate the operating conditions of the PCB. This stresses the vias and by monitoring the changes in resistance can determine the expected life of the product based on design rules, manufacture standard and quality of the process. Although the testing and reliability of a particular set

Figure 1 - Typical examples of via connections

Figure 2 - Traditional section and Copper foil separation (left); separation between the Copper pad and the inner Copper barrel (middle); separation between the Copper pad and the inner Copper barrel at a higher magnification (right)



of coupons can be determined, final assessment of the failure mode requires a microsection.

Over the last year experience has been gained in using a different approach, or perhaps just coming at the problem from a different angle. Over many years engineers have produced traditional microsections looking at plated through holes along the length of the barrel. In the case of multilayer boards if any concerns were seen on barrel plating and inner foil separation, experienced engineers would turn the section around and examine the Copper pad connection.

The images in Figure 2 show a traditional section and Copper foil separation. The second image shows the Copper pad and the inner Copper barrel separated, the third image is at a higher magnification. This is achieved by grinding the section up through the barrel and illustrates if complete or only partial separation is present.

Back grinding of section has also been used on board assemblies to look at voiding, solder shorts and corrosion under chip components. Figure 3 shows solder shorting and voiding under the chip component when viewed from under the pads.

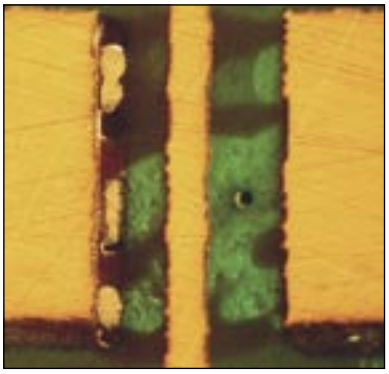


Figure 3 - Solder shorting and voiding under a chip component when viewed from under the pads

Examination of blind vias by back grinding

The following procedure may be used to examine blind via hole interconnections for routine testing or during failure analysis of a printed circuit board. The illustrations outline the typical procedure and the information that may be obtained from any via.

A section of the board must be cut containing the via or group of via holes under examination. This can be conducted with a rotary saw to minimise damage to the board or flexing thin substrates. Examination of the Gerber files can help to determine the points of interest provided the fault locations have been determined by electrical test. The design files can also show other via positions in this particular layer.

The board section must be cleaned in IPA to remove any surface contamination. This also ensures the mounting resin will adhere correctly during curing. The section of the board must be marked or a reference diagram/photograph made so the correct via or vias are being examined at all times.

The board section is then placed in a microsection mould. The position must be such that the back of the via or capture pad is facing down. The epoxy mix must be poured in slowly to cover and surround the section of the circuit board. The epoxy is simply being used to hold the board during the grinding operation.

The section mould must be placed in an air circulated oven and the epoxy allowed to cure. When the epoxy is fully cured it is carefully removed from the mould and the exposed face of the board towards the back of the via hole capture pad must be ground. Grinding can be conducted initially using a 400 grit then reducing to a 600 grit paper to slow down the epoxy removal rate. Scratches are not really an issue in this procedure but control of the depth is more important. Figure 4 shows examples of via and track patterns visible through the PCB during grinding.

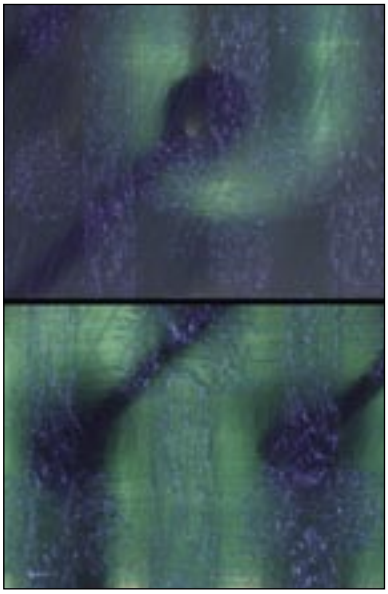


Figure 4 - Examples of via and track patterns visible through the PCB during grinding

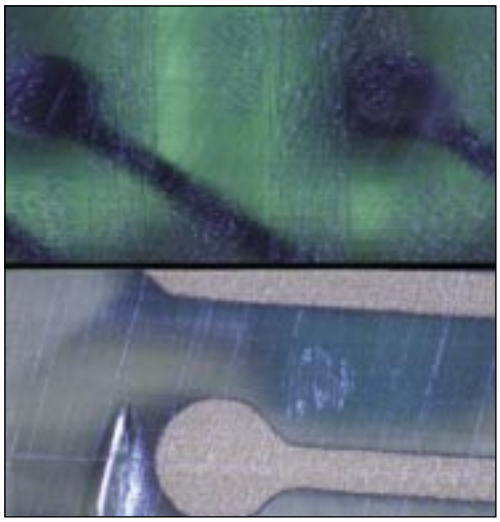


Figure 5 - Tracks leading to the blind via capture pads (above) and a close up of pad just below the Copper foil (below)

The depth of grinding must be checked regularly with a microscope or 20x eye glass to determine when the pad surface is near. Ideally the objective is to reach the base Copper foil surface or the epoxy layer just below the Copper track and pad. With care, and keeping the section flat, it should be possible to examine more than one via

interconnection using this technique. If more than one via can be examined then a better understanding of the quality of the interconnection can be made. If this technique is only being used for failure analysis of a specific via other vias can be examined first without disturbing the via in question. They allow an engineer unfamiliar with the technique to practice.

The images in Figure 5 show tracks leading to the blind via capture pads (above) and a close up of pad just below the Copper foil (below). Figure 6 shows one track cut in preparation to via pad removal (above) and a second one prior to cutting the track between via pad and through hole via (below).

When the section to the base of the Copper foil has been ground, it must be placed under a microscope and the track end connected to the capture pad probed. The track must then be peeled from the surface of the epoxy. If during grinding the Copper surface is not reached, far less strain will be put on the track and Copper pad during peeling. When the Copper track is peeled back, the capture pad will also be separated from the base of the plated via. Figure 7 shows a close up of a via pad after removal (left), the surface of the Copper under the via hole (middle) and a close up of the Copper surface (right).

The track and connected pad can now be placed in a sealed container for future examination, also the section can be placed in another sealed container. Correct storage of the samples prevents any debris falling on the two surfaces and possibly confusing any future analysis.

Both of the mating surfaces of the blind via that have been separated can be carefully examined. First examination is conducted with a high magnification microscope to look at the previously mating surfaces. It should be possible to compare the surface of each and show how they have separated, if the Copper plating to the pad was defective or not. The two surfaces should have features that match like two jigsaw pieces.

Using an SEM, images can be taken of both mating surfaces. A mechanical break between two Copper surfaces should provide a distinctive pattern allowing comparison on both surfaces. If the vias were correctly formed with a sound metallurgical bond but failed due to assembly or rework conditions, a hard fracture would be noted.

If the quality of the plating, hole and pad surface preparation was poor, then surface analysis on an SEM should be able to identify and characterise any contamination. It could then compare with the surrounding materials used in the fabrication process.

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Figure 6 - One track cut in preparation to via pad removal (above) and a second one prior to cutting the track between via pad and through hole via (below)

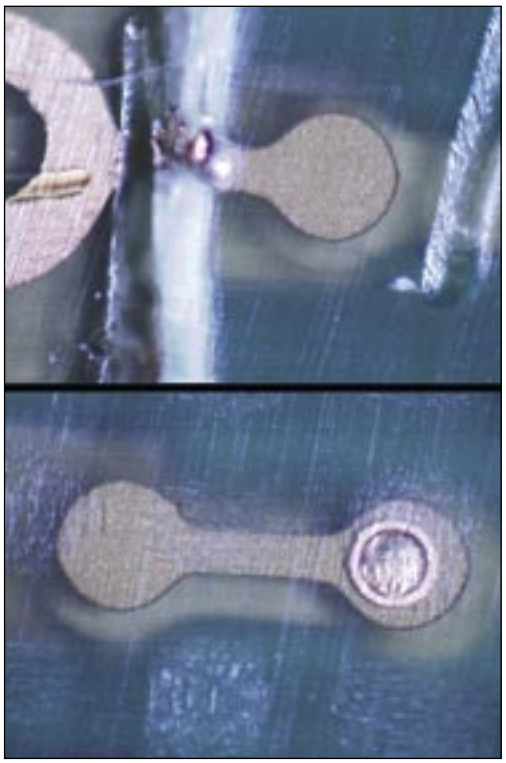

Figure 7 - Close up of a via pad after removal (left), the surface of the Copper under the via hole (middle) and a close up of the Copper surface (right)

Figure 8 - The two SEM images show the surface of the 0.020" 0.5mm capture pad (left) after separation from the bottom of the 0.010" 0.25mm blind via (right). There is no evidence of a fractured surface suggesting that a true bond could not have formed during the blind via plating process. Although no measurement of the force to remove the capture pad has been made, the bond was noticeably weaker than pads of the same size on known good vias