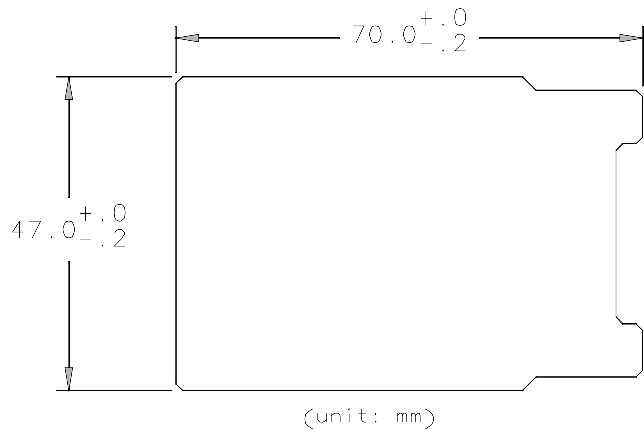
# B-2382 V3.2C Specification Drawing




## BOARD's DRILL SCHEDULE (unit: inch)

| DRILL SYMBOL | DRILL SIZE | COUNT | PLATED | Min/Max |
|---|---|---|---|---|
| ○ | .015 | 228 | YES | --- |
| ⊞ | .02 | 2 | YES | --- |
| ⦶ | .028 | 3 | YES | --- |
| ⊟ | .035 | 46 | YES | --- |
| ⊖ | .041 | 6 | YES | --- |
| ◫ | .059 | 6 | YES | --- |

## B-2382 V3.2C PC BOARD SPECIFICATIONS

1. Board Layers: 8
2. Layer Stack Order:
   - Layer1: Top component layer(signal_1).
   - Layer2: Power plane(Vcc, AVCC).
   - Layer3: Inner signal layer(signal_3).
   - Layer4: Power plane (AGND).
   - Layer5: Power plane (GROUND).
   - Layer6: Inner signal layer(signal_4).
   - Layer7: Power plane (VEE,VCC2).
   - Layer8: Bottom component layer(signal_2).
3. Apply silkscreen on both side:
   - Film9: Top component side silkscreen.
   - Film10: Bottom component side silkscreen.
4. Apply solder mask over bare copper on both side:
   - Film11: Top component side solder mask.
   - Film12: Bottom component side solder mask.
5. Material: FR4.
6. Board thickness: 0.062'' +/- 0.010.
7. Board outline is metric
8. All layers are equal thickness.
9. Copper thickness 1oz before plating.
10. All dimensions are in inches unless otherwise noted.

11: Contact person:


Fukun Tang/Electronics Engineer
Electronics Development Group
University of Chicago
Tel: (773)-702-7801, Fax: (773)-702-2971


Note: Rev. v3.2c interchanges label for layer 4 and layer 5 in Item 2 (layer stock order) above.

SCHM# B-2381 v3.2c
SPEC# B-2382 v3.2c
ASSM# B-2383 v3.2c

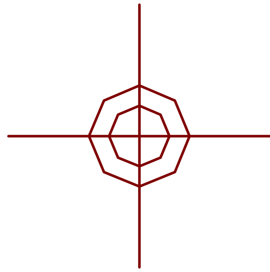
UNIVERSITY OF CHICAGO
ELECTRONICS DEVELOPMENT GROUP

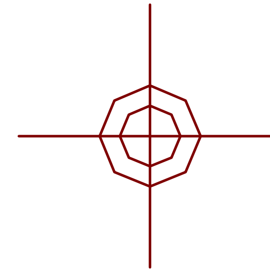
TITLE
B-2382 V3.2 Specification Drawing

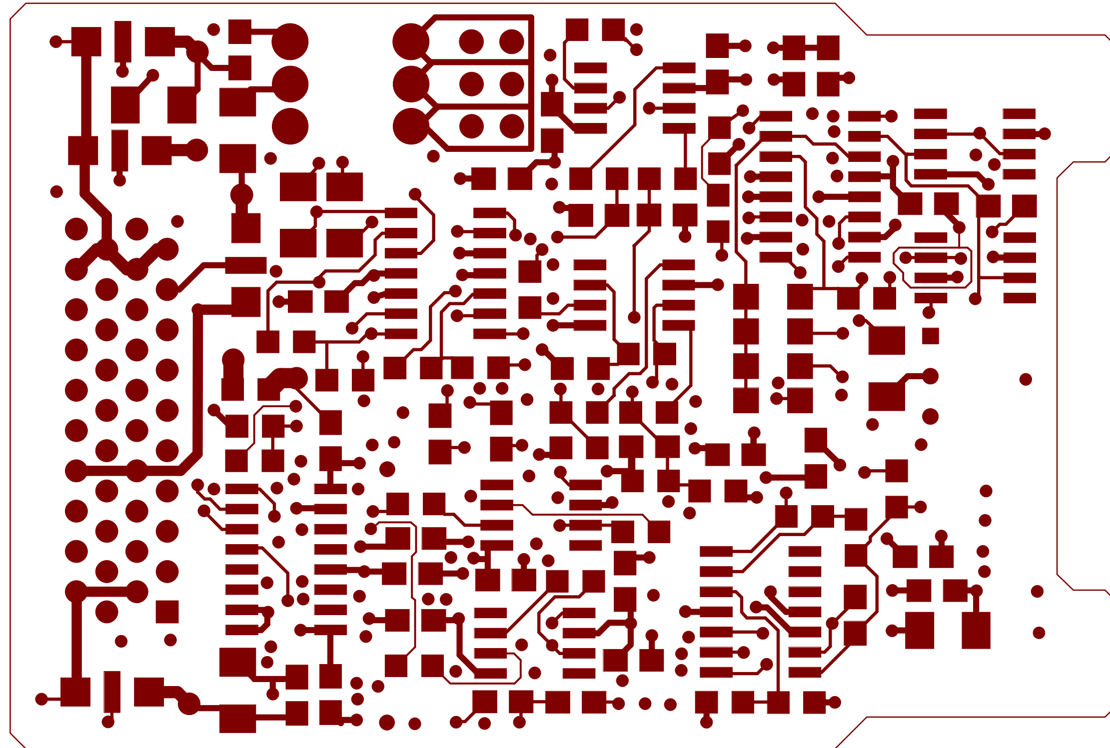
SHEET 1 OF 1
DATE 4/11/00
DRAWN TANG

B- 2382
REV V3.2c

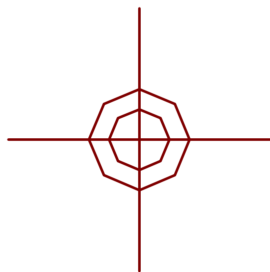
Pcgerber II V 6.0 : Fri Oct 08 14:32:13 1999 - 2382v32.pcb : artwork_1







Film1: LAYER1 (Top layer, SIGNAL_1)



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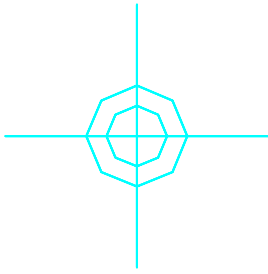
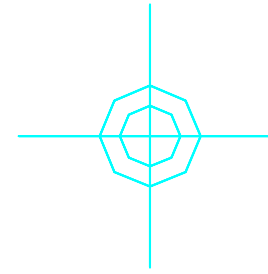
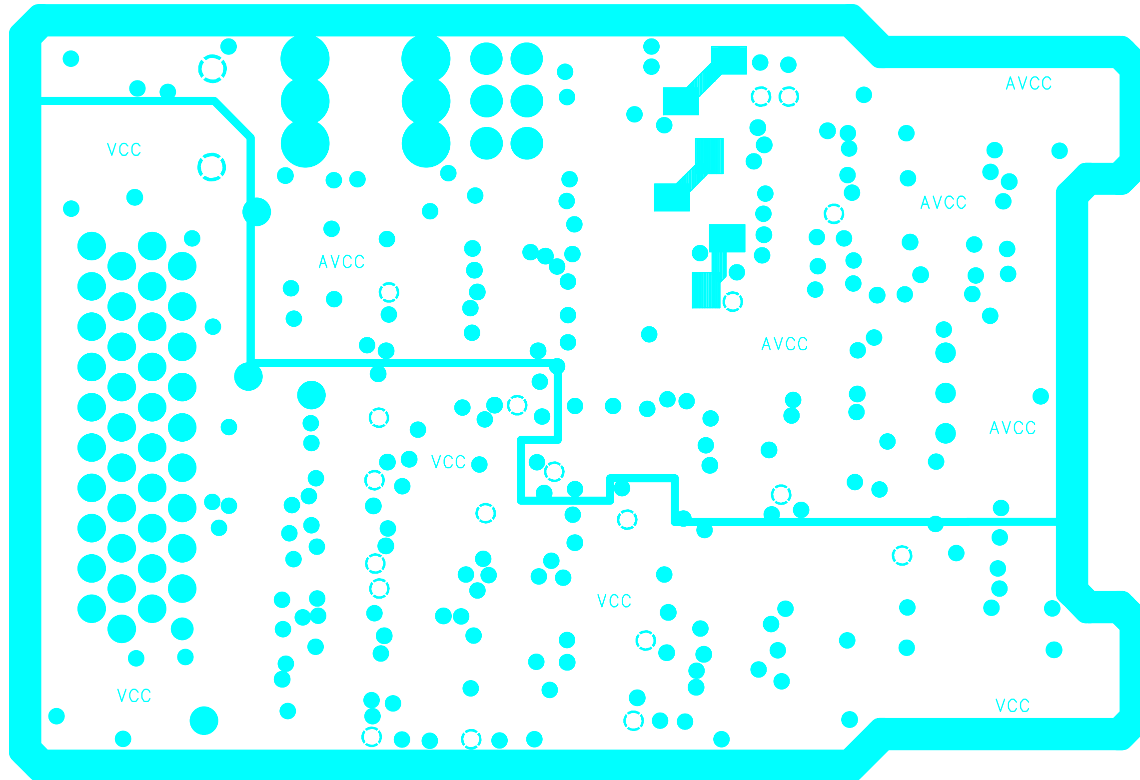
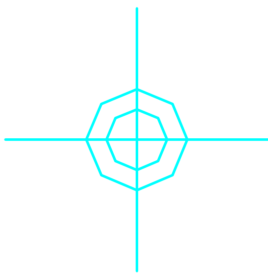







FILM2: LAYER2 (VCC,AVCC)



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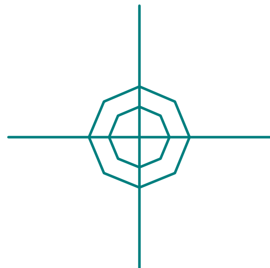
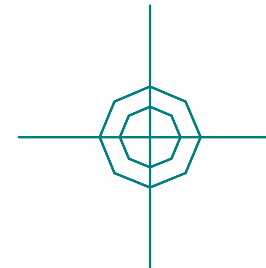
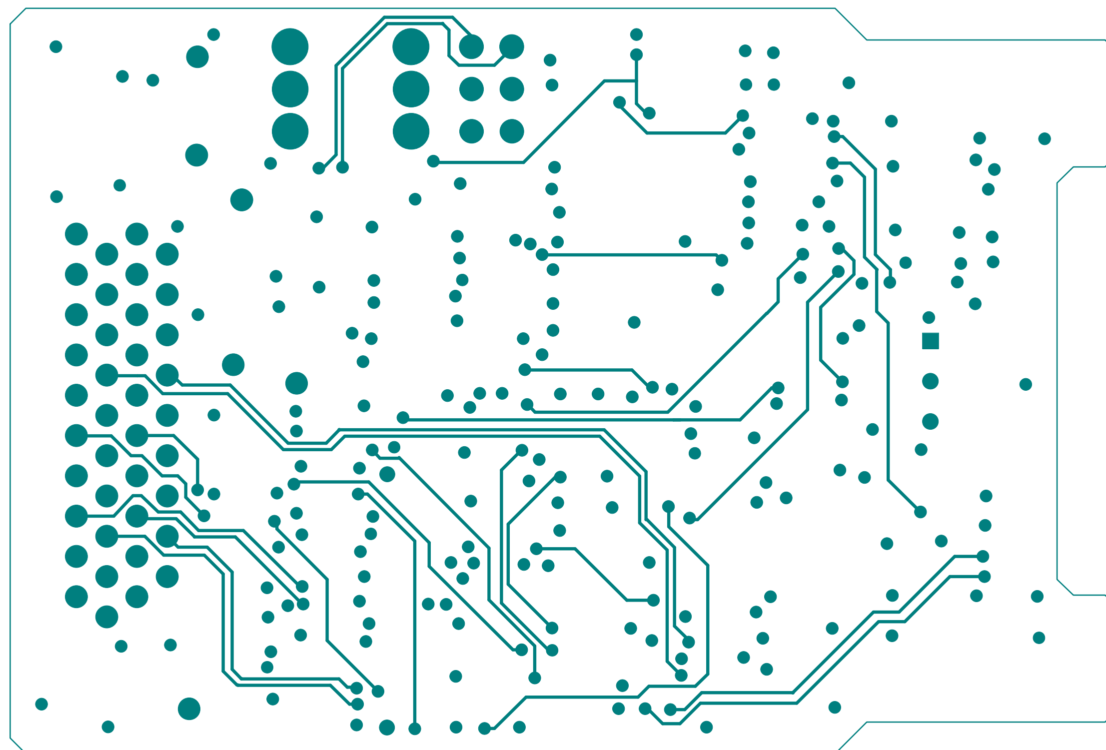
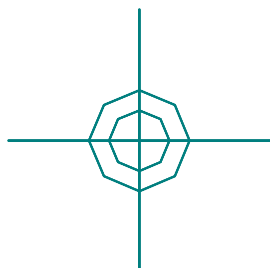






FILM3: LAYER3 (inner signal layer1, SIGNAL_3)



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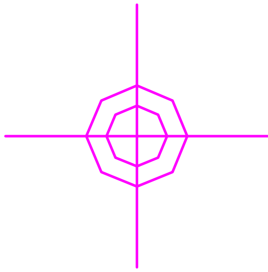
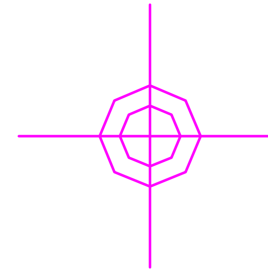
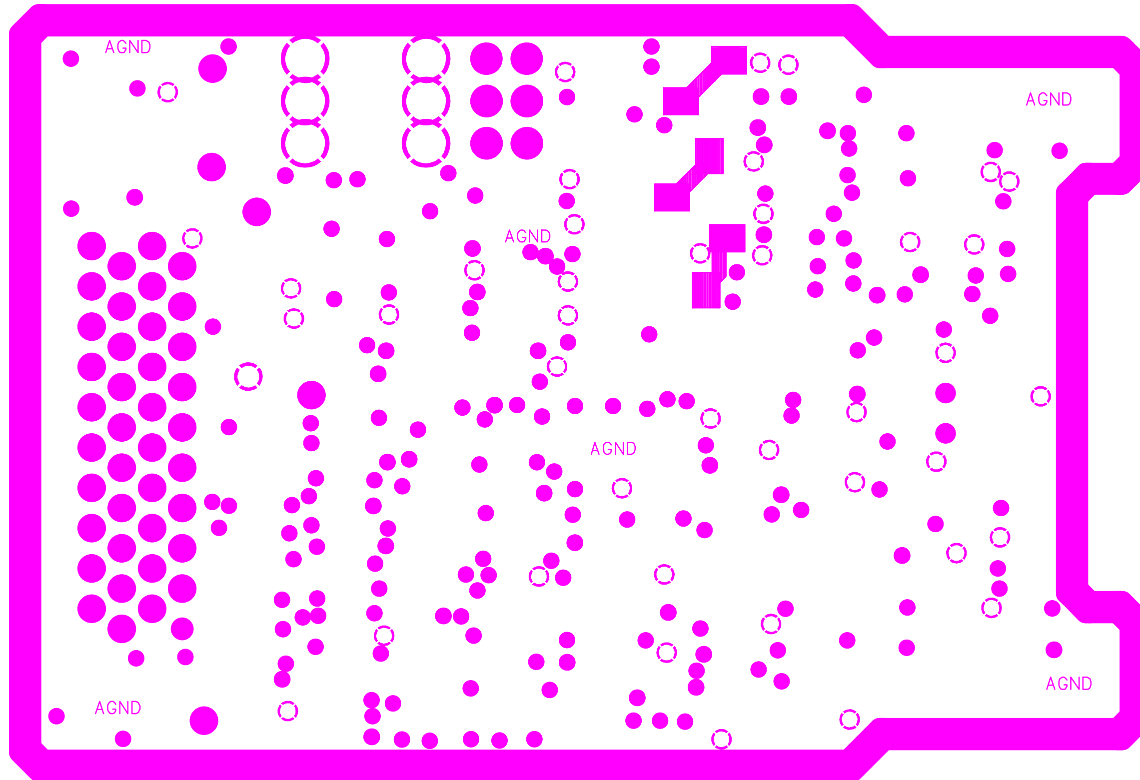
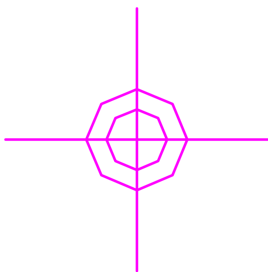







FILM4: LAYER4 (AGND)



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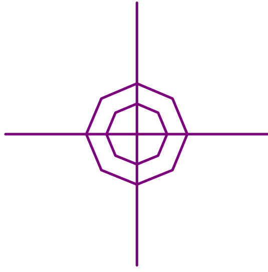
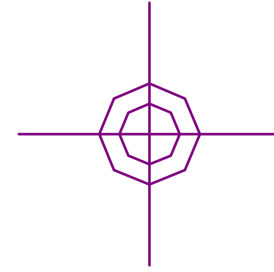
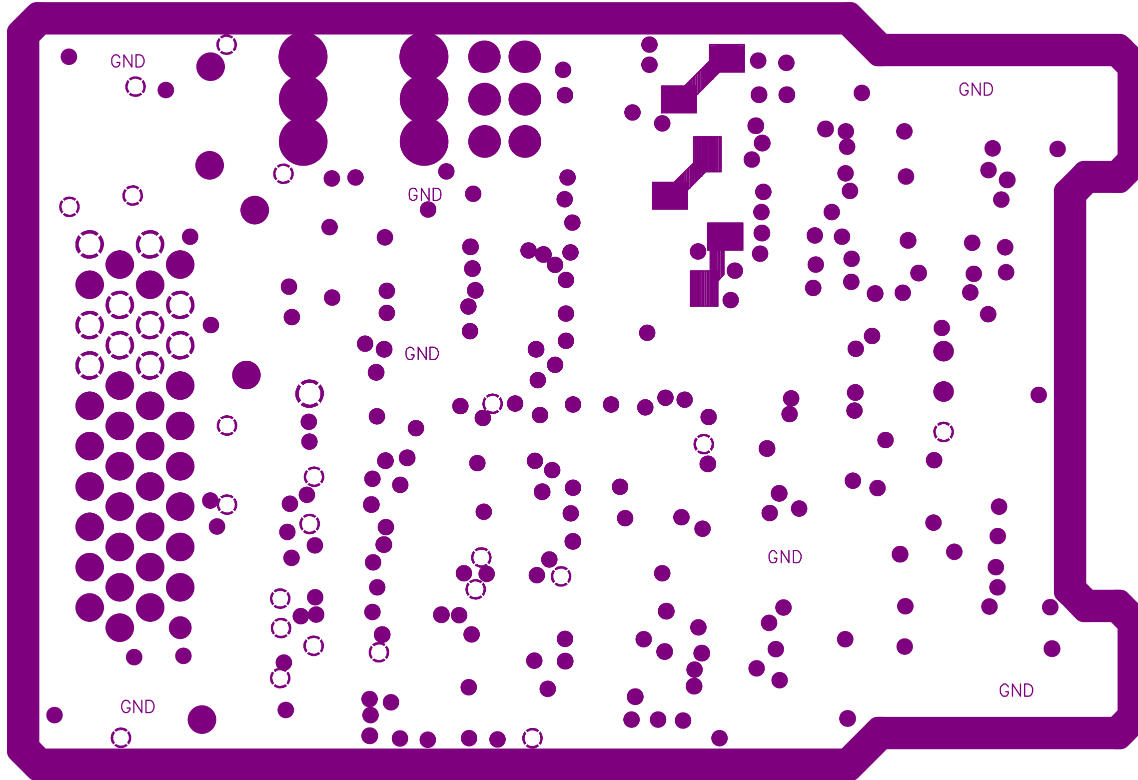
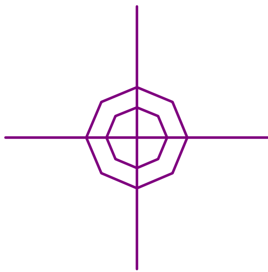
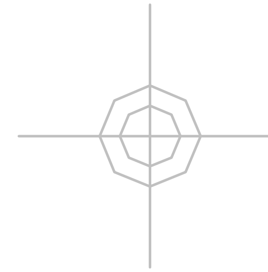


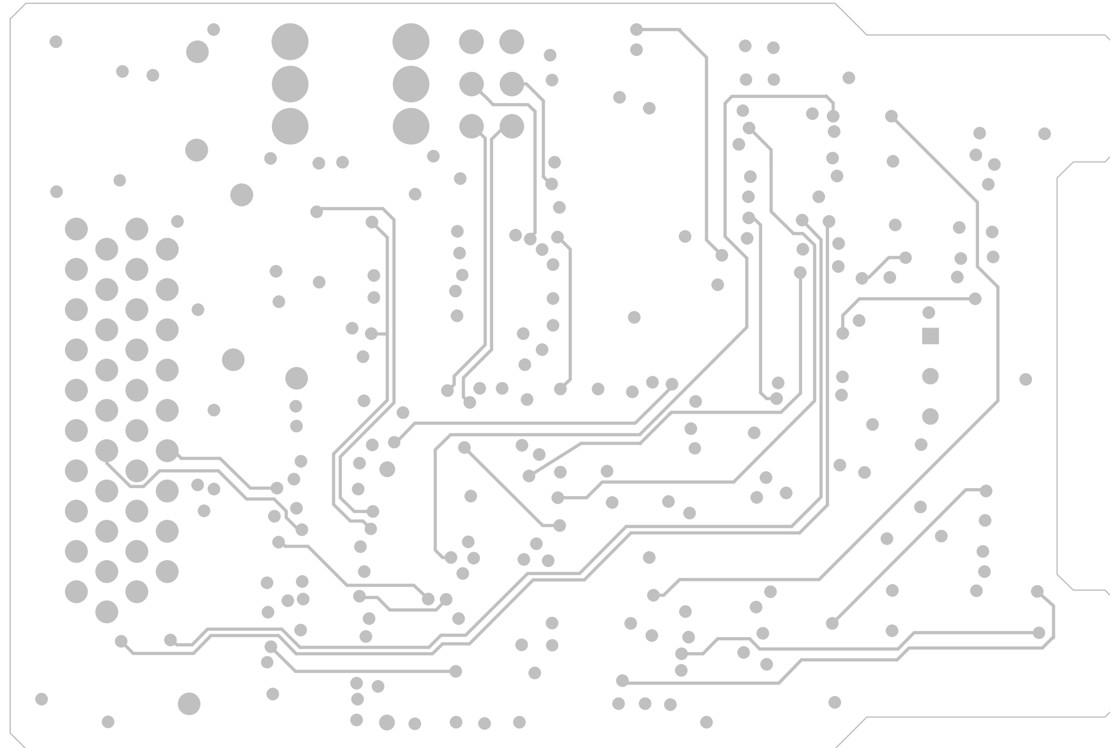





FILM5: LAYER5 (GROUND)







FILM6: LAYER6 (inner signal layer2, SIGNAL_4)

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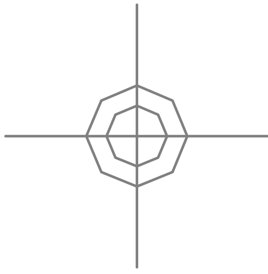
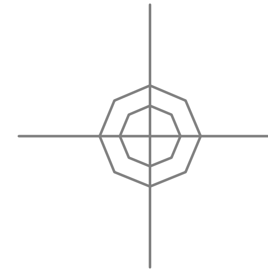
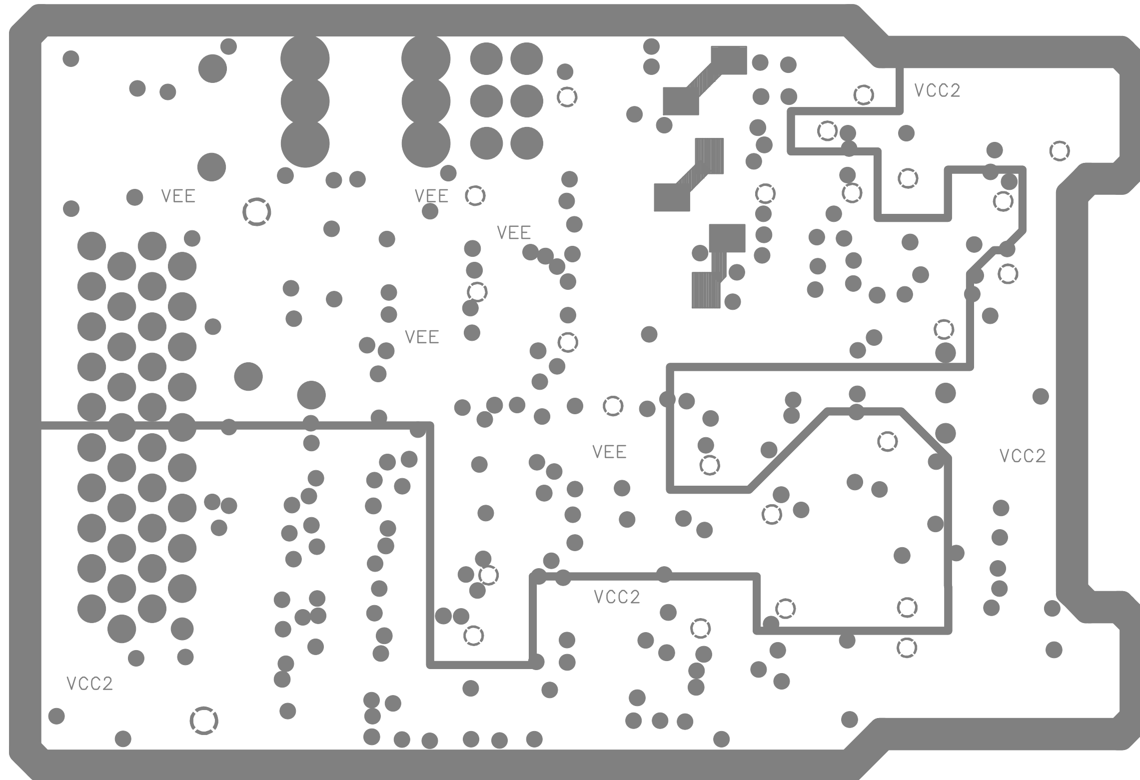
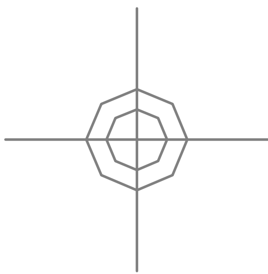







FILM7: LAYER7 (VEE,VCC2)



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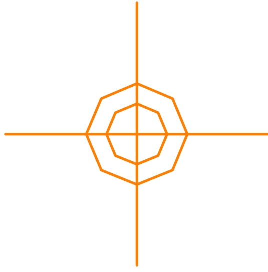
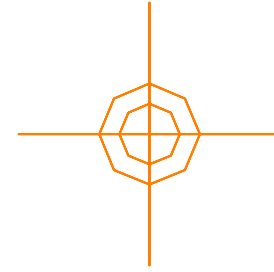
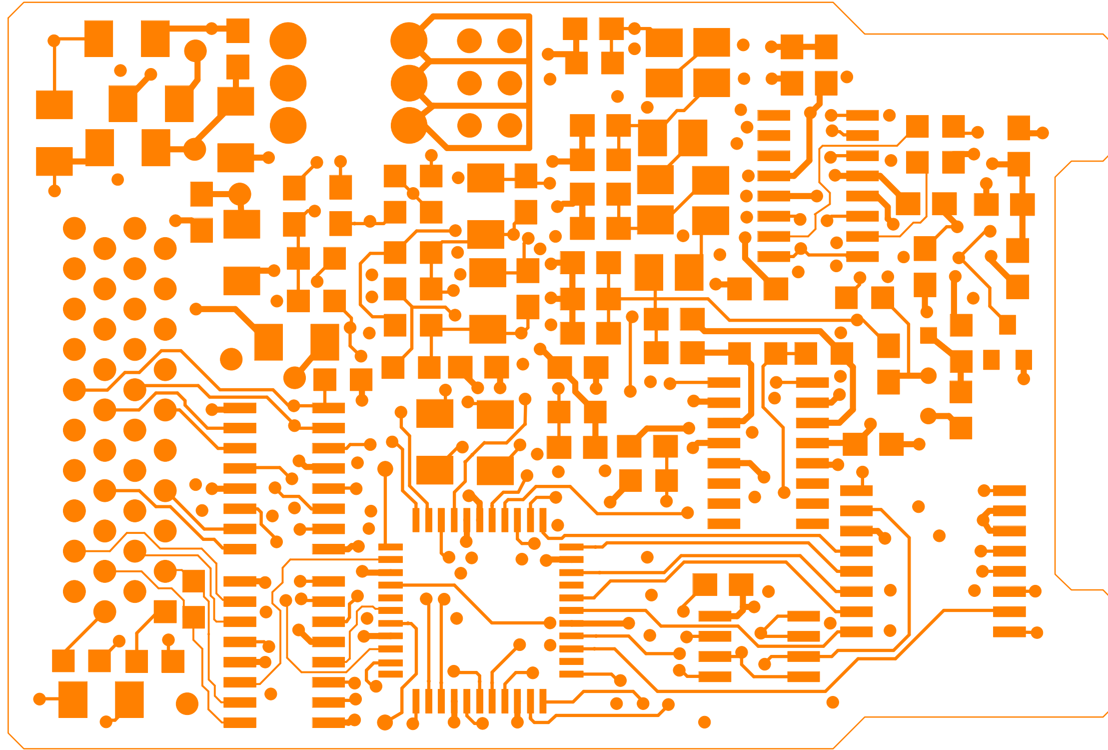
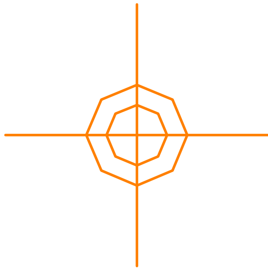






FILM8: LAYER8 (Bottom layer, SIGNAL_2)



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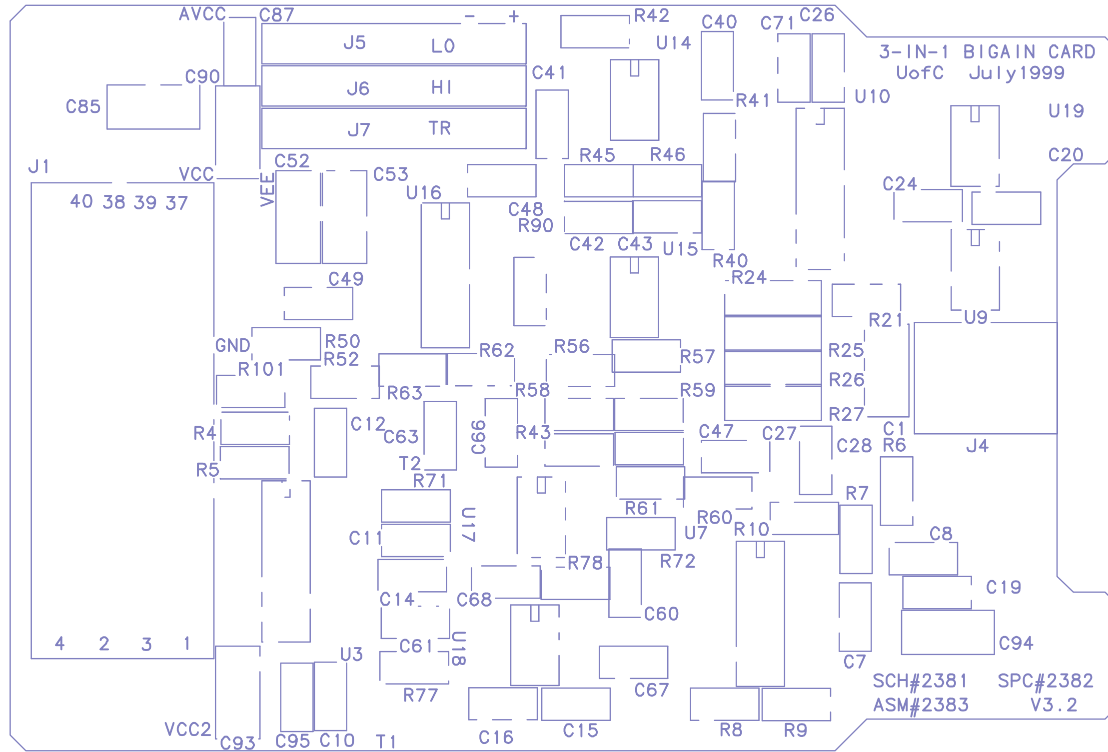
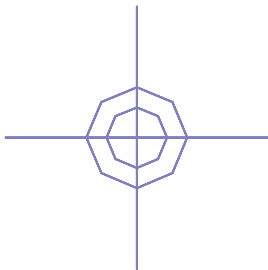



FILM9: Top Silkscreen (SILK_SCREEN_1)



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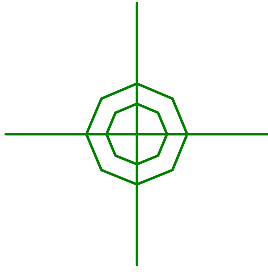
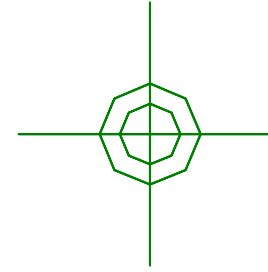
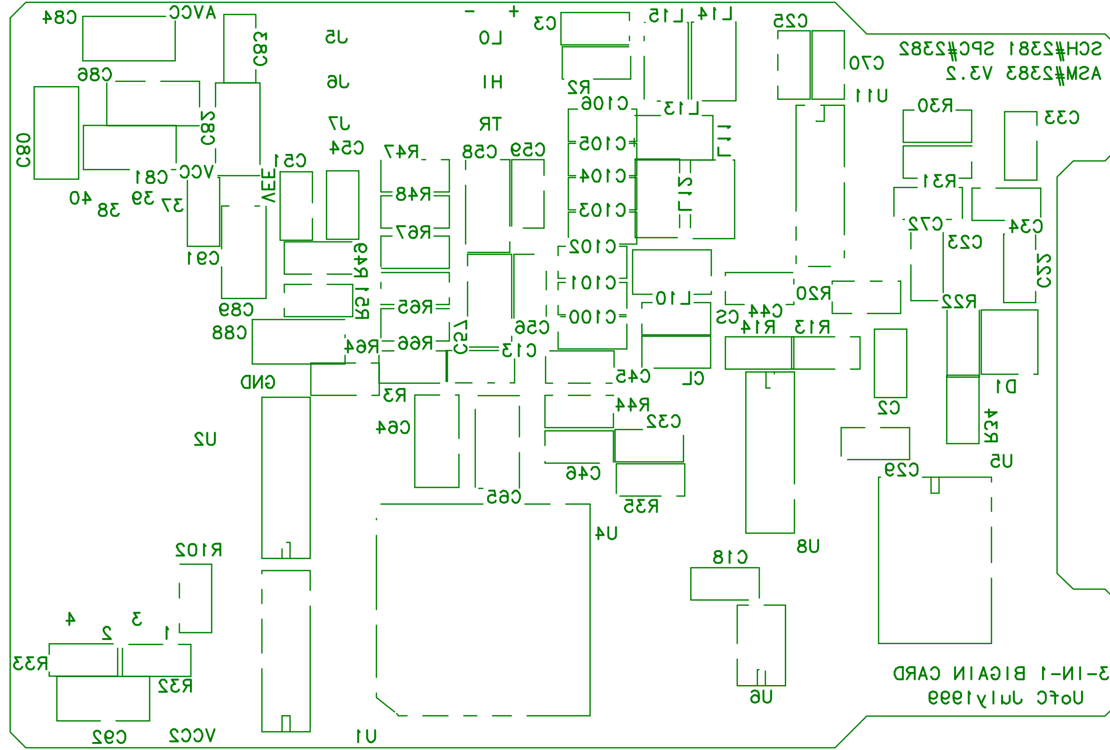
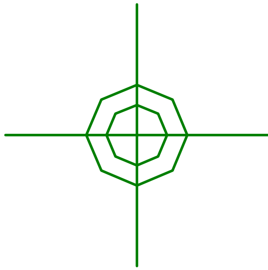
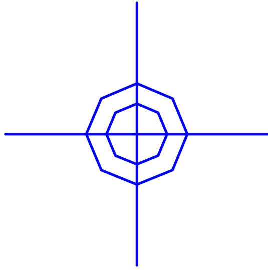


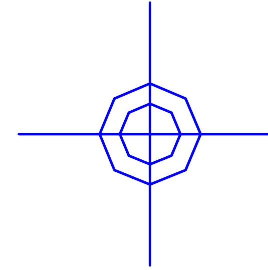


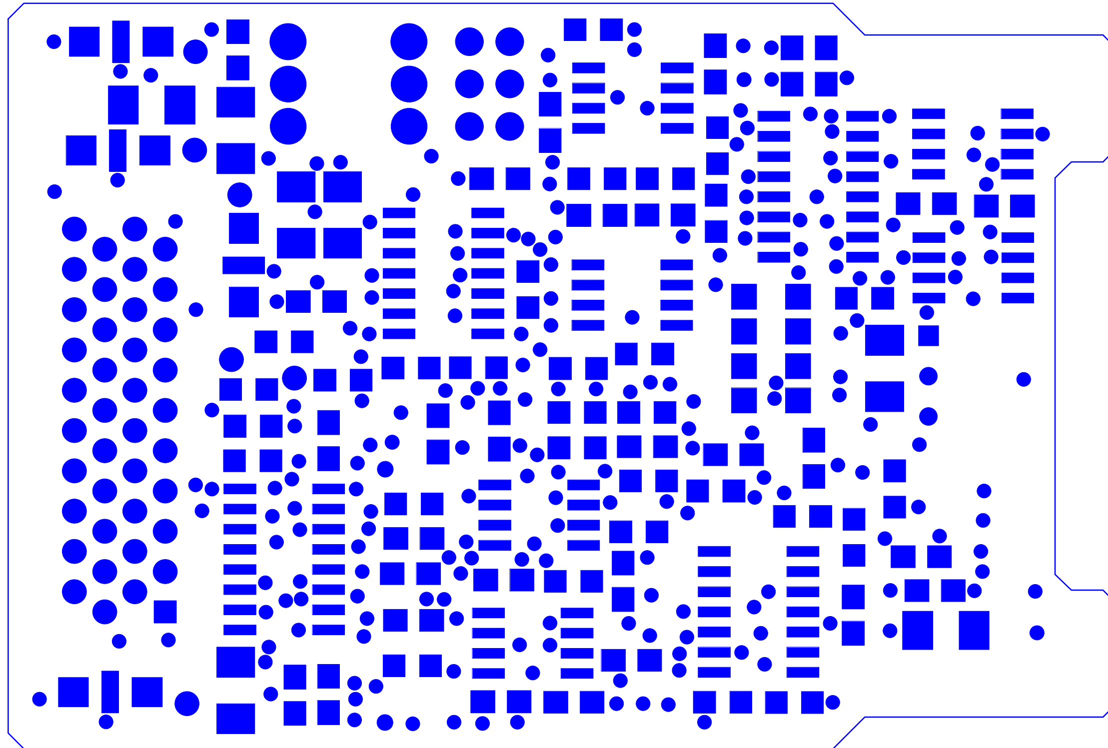


FILM10: Bottom Silkscreen (SILK_SCREEN_2)

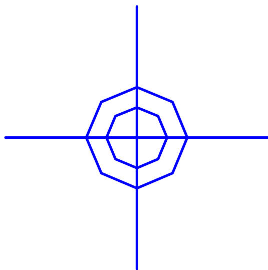








FILM11: Top Solder Mask (SOLDER_MASK_1)



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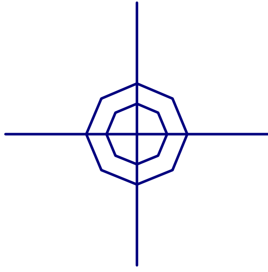
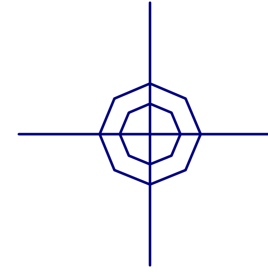
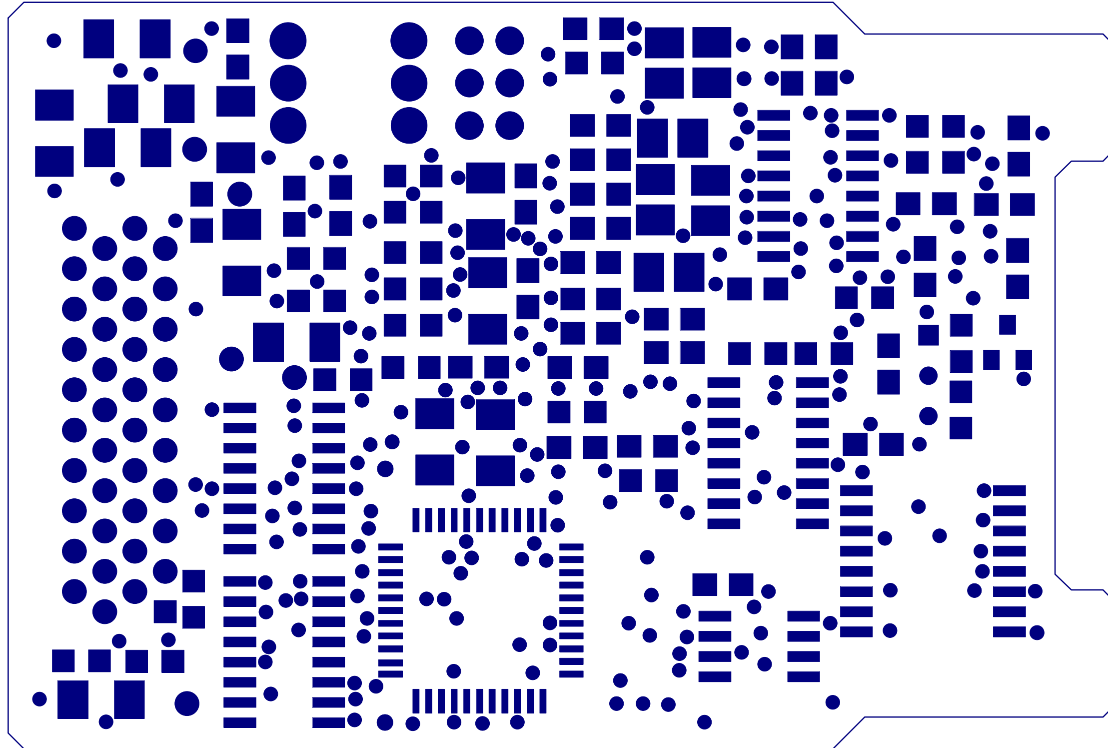
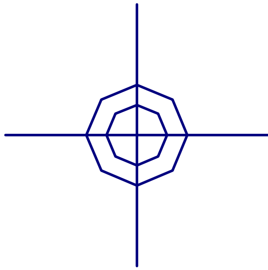






FILM12: Bottom Solder Mask (SOLDER_MASK_2)



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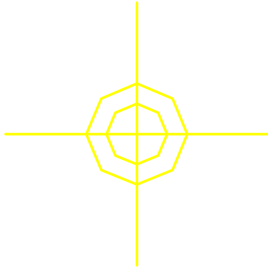
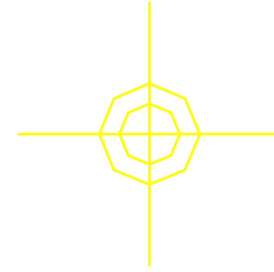
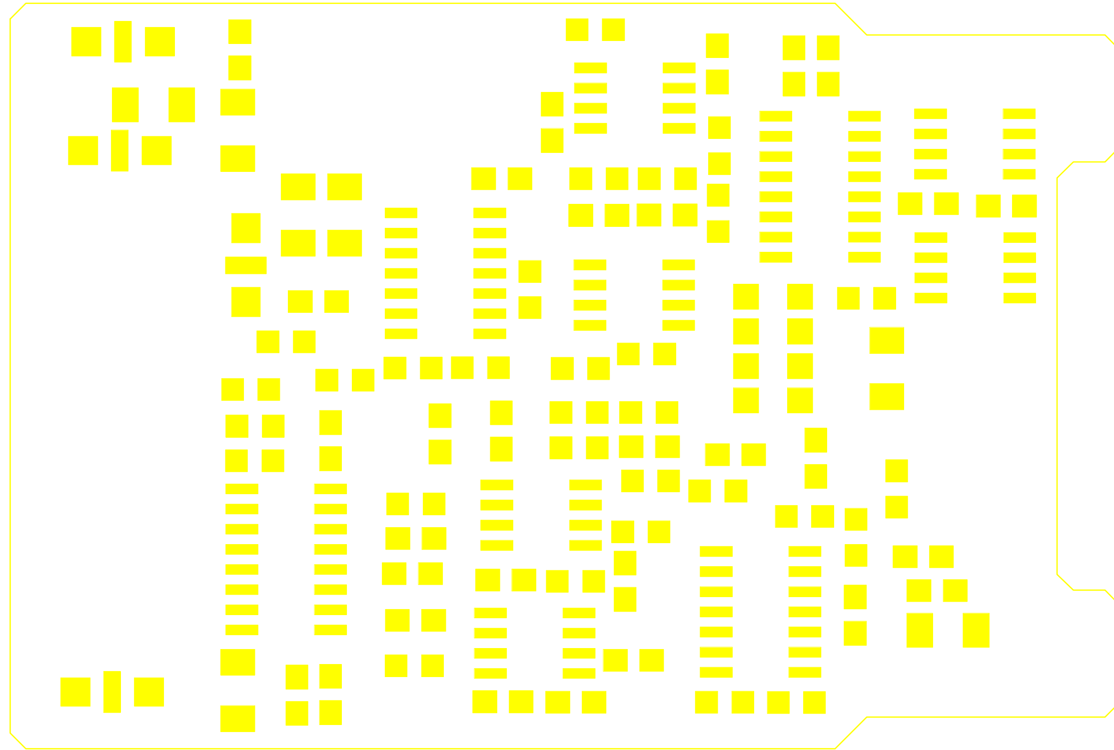
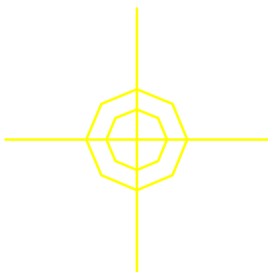






FILM13: Top Paste Mask (PASTE_MASK_1)



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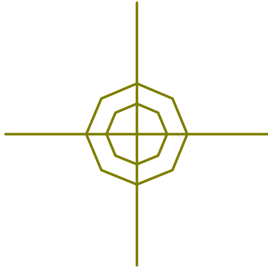

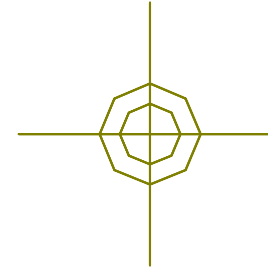

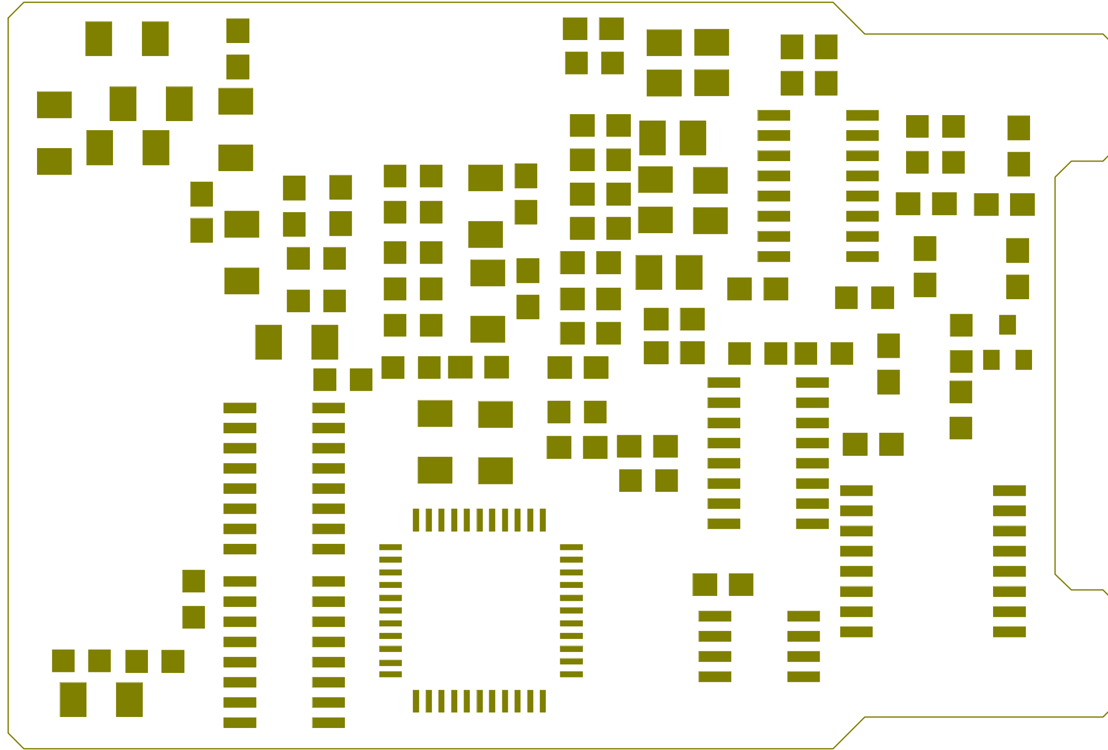

FILM14: Bottom Paste Mask (PASTE_MASK_2)