PADS PCB Design Solutions

PCBs en Aplicaciones Espaciales

CSIC

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Introducción

Visión de Conjunto

Consideraciones para el Diseño PCB

Condiciones de
- Diseño eléctrico
- Diseño mecánico
- Diseño térmico

Ejemplos de diseños realizados y en curso en el IAA

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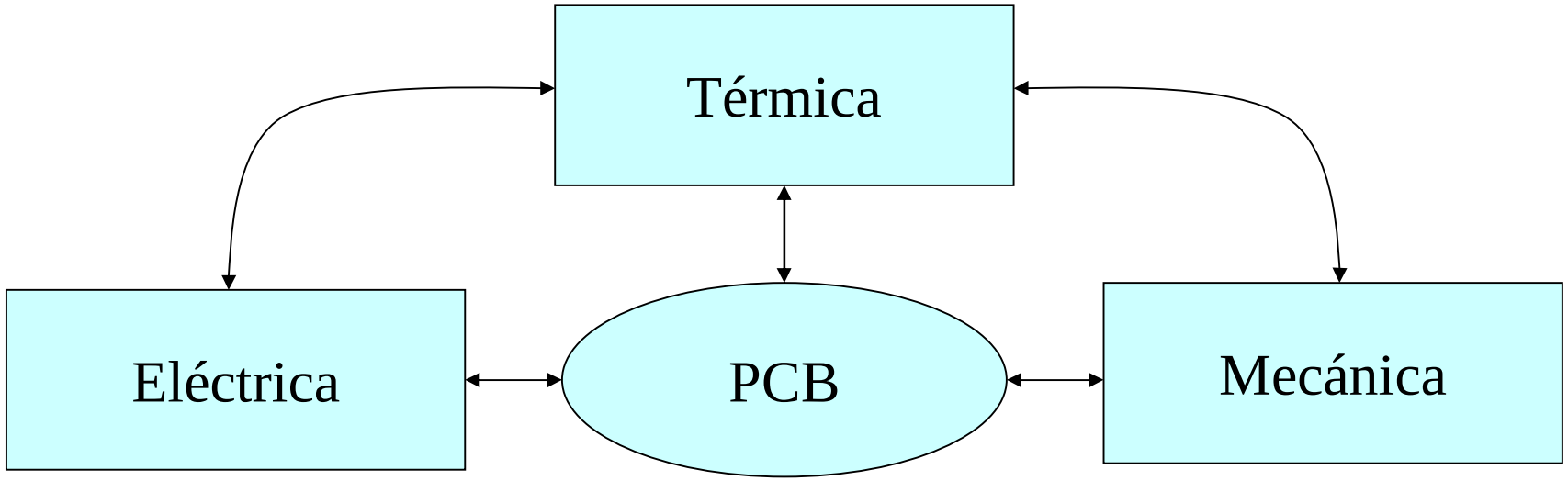
Visión de Conjunto



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Condiciones de diseño eléctrico

Requerimientos Funcionales

Filosofía de modelos (STM, EQM, QM, FM, FS)

Recopilación información y Búsqueda componentes (QPL's, PPL's, MIL's)

Compatibilidad electromagnética (Grounding & Bonding EMI Filter)

MIL-STD-461C, CS01, CS02, CE03
MIL-STD-461D, CE102

Diseño del esquema

Elementos y caminos críticos, Análisis de fallos

ECSS-Q-30-02 Failure modes, effects and criticality analysis (FMECA)

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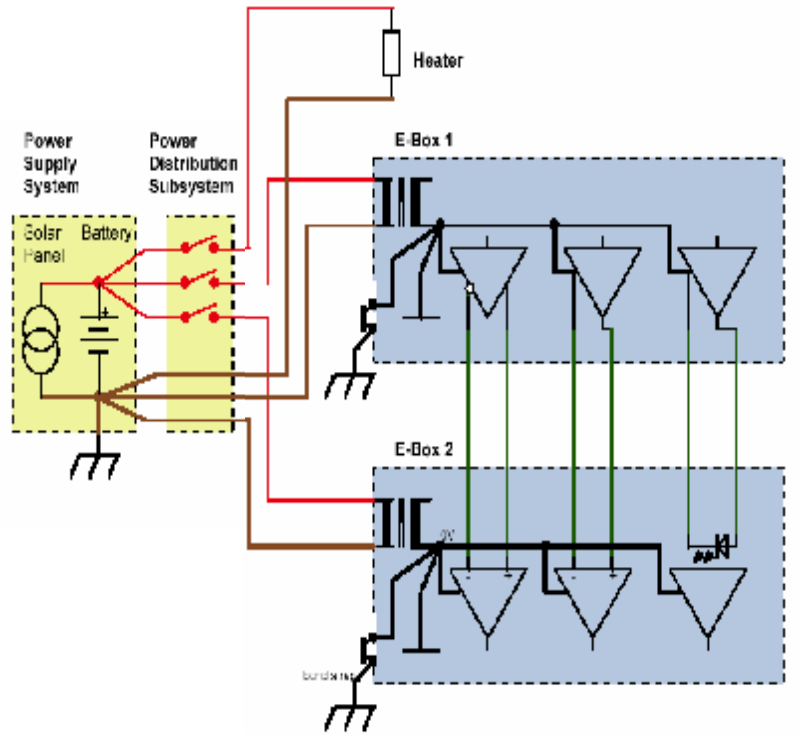
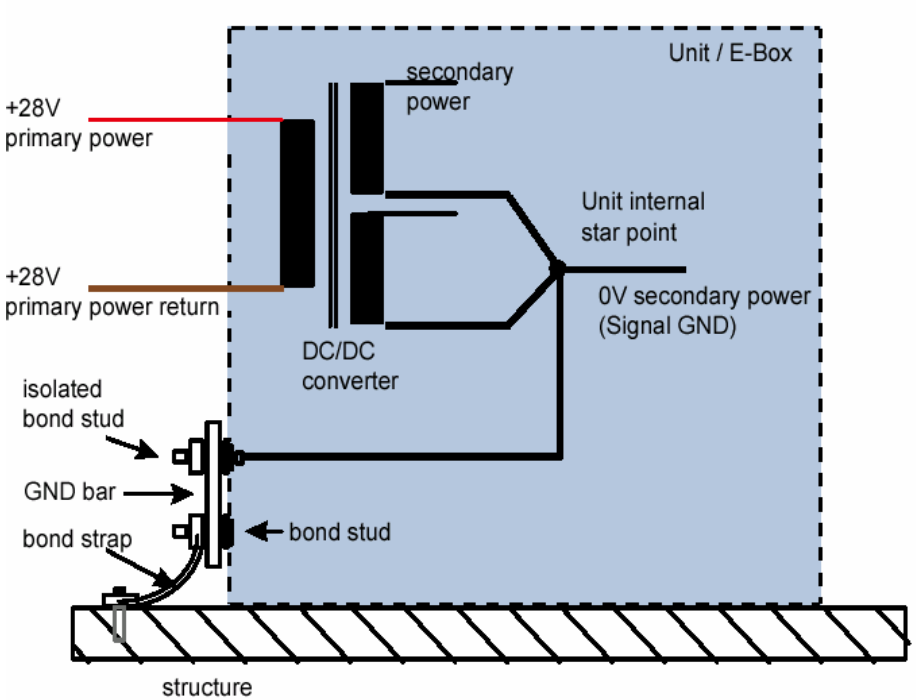
Grounding and Bonding





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C

American Environments
MIL-STD-461A, MIL-STD-461B and MIL-STD-461C Capabilities

Conducted Emissions

Test Method	Frequency Range	Details
CE01	30Hz to 15kHz	Power & Interconnecting Leads
CE03	15kHz to 50MHz	Power & Interconnecting Leads
CE06	10kHz to 26GHz	Antenna Leads
CE07	Spikes	Power Leads

Conducted Susceptibility

Test Method	Frequency Range	Details
CS01	30Hz to 50kHz	Power Leads
CS02	15kHz to 400MHz	Power Leads
CS03	15kHz to 10GHz	Intermodulation
CS04	30Hz to 20GHz	Signal Rejection
CS05	30Hz to 20GHz	Cross Modulation
CS06	Spikes	Power Leads
CS07		Squelch Circuits
CS09	60Hz to 100kHz	Structure Current, Common Mode
CS10	10kHz to 100MHz	Damped Sinusoids Pin Injection
CS11	10kHz to 100MHz	Bulk Current Common Mode

Radiated Emissions

Test Method	Frequency Range	Details
RE01	30 Hz to 50kHz	Magnetic Field
RE02	14kHz to 10GHz	Electric Field
RE03	Spurious & Harmonics	Antenna Leads

Radiated Susceptibility

Test Method	Frequency Range	Details
RS01	30Hz to 50kHz	Magnetic Field
RS02	Spikes & Power Frequency	Magnetic & Electric Fields
RS03	14kHz to 40GHz	Electric Field
RS05	EMP	

American Environments
MIL-STD-461D and MIL-STD-461E Capabilities

Conducted Emissions

Test Method	Frequency Range	Details
CE101	30Hz to 10kHz	Power Leads
CE102	10kHz to 10MHz	Power Leads
CE106	10kHz to 40GHz	Antenna Terminal

Conducted Susceptibility

Test Method	Frequency Range	Details
CS101	30Hz to 150kHz	Power Leads
CS103	15kHz to 10GHz	Intermodulation, Antenna Port
CS104	30Hz to 20GHz	Signal Rejection, Antenna Port
CS105	30Hz to 20GHz	Cross Modulation, Antenna Port
CS109	60Hz to 100kHz	Structure Current
CS114	10kHz to 200MHz	Bulk Cable Injection
CS115	Impulse	Bulk Cable Injection
CS116	10kHz to 100MHz	Damped Sine, Cables and Power Leads

Radiated Emissions

Test Method	Frequency Range	Details
RE101	30 Hz to 100kHz	Magnetic Field
RE102	10kHz to 18GHz	Electric Field
RE103	10kHz to 40GHz	Antenna Spurious & Harmonic Outputs

Radiated Susceptibility

Test Method	Frequency Range	Details
RS101	30Hz to 100kHz	Magnetic Field
RS103	2MHz to 40GHz	Electric Field
RS105	Transient	Electromagnetic Field

MIL-STD-461C

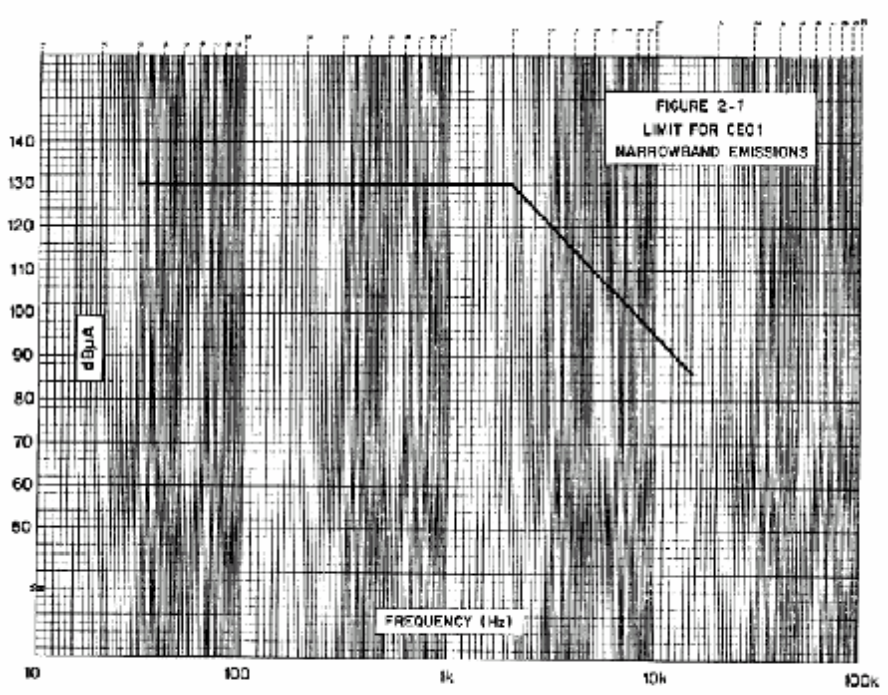


FIGURE 2-1. LIMIT FOR CE01 NARROWBAND EMISSIONS

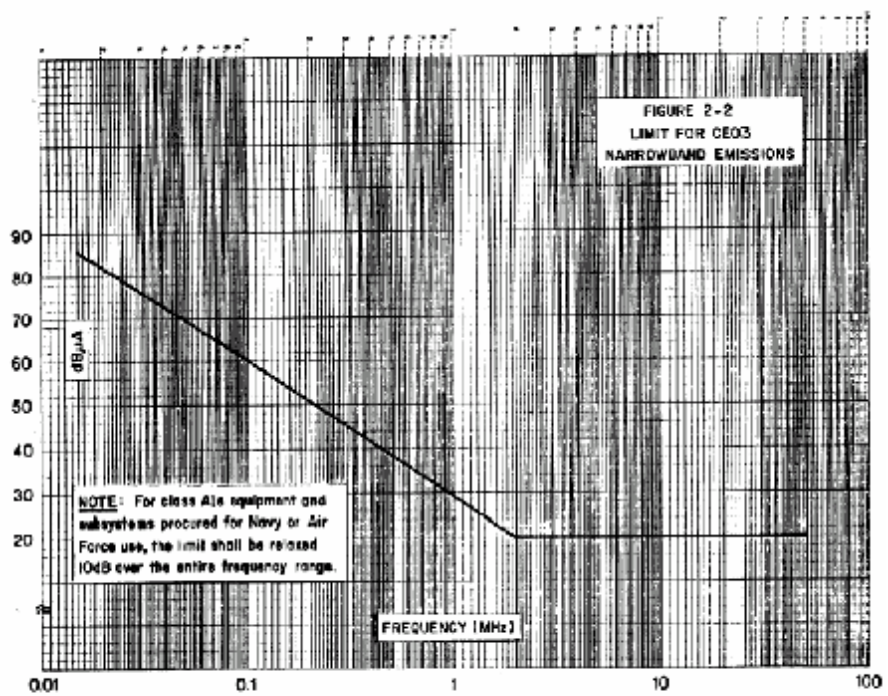


FIGURE 2-2. LIMIT FOR CE03 NARROWBAND EMISSIONS

MIL-STD-461C

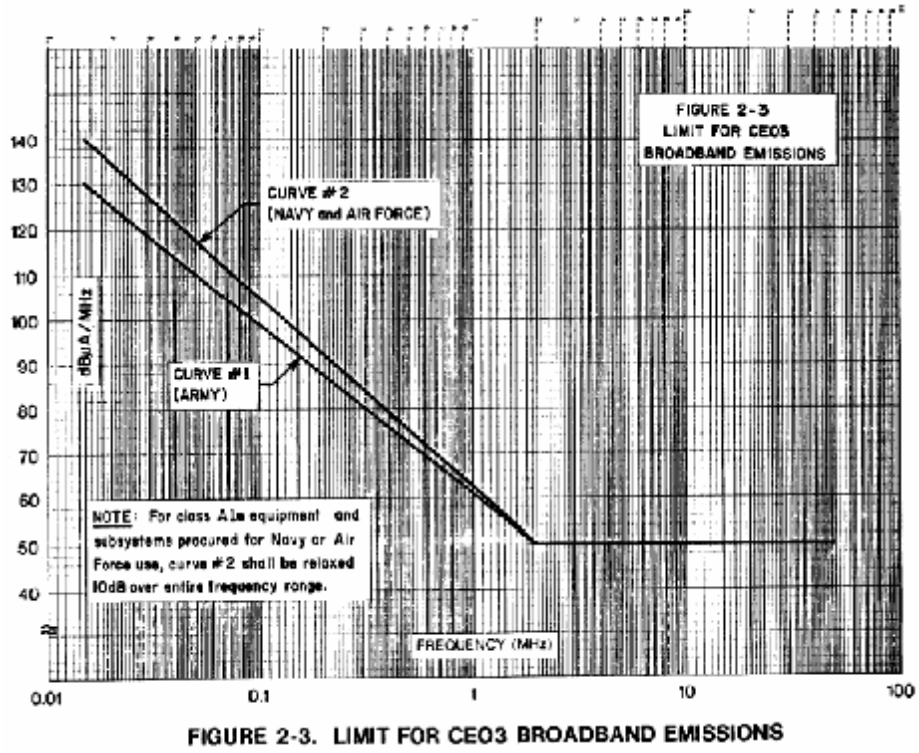


FIGURE 2-3. LIMIT FOR CE03 BROADBAND EMISSIONS

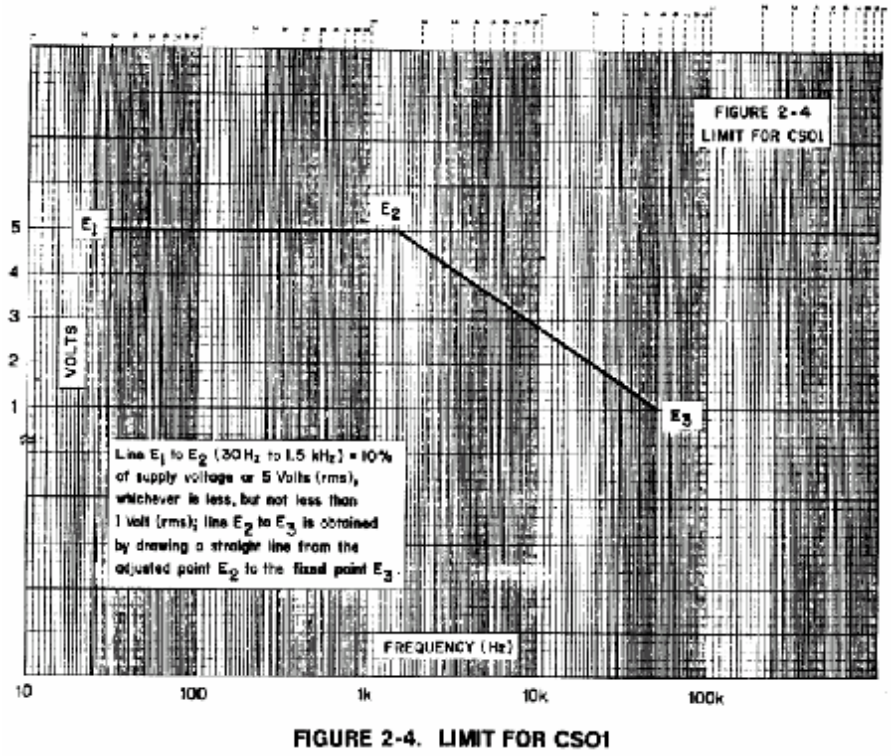
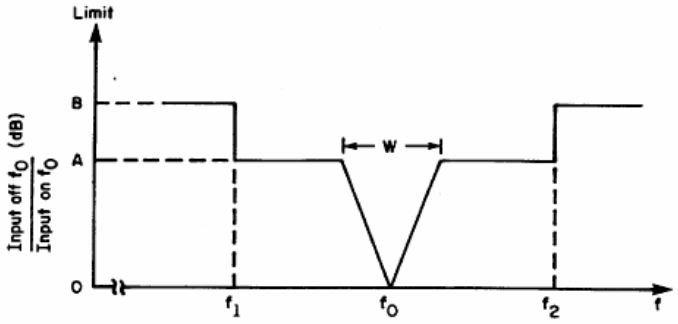


FIGURE 2-4. LIMIT FOR CS01

MIL-STD-461C



f_0 = Receiver tuned frequency or band center for amplifiers.

f_1 = Lowest tunable frequency of receiver band in use or the lowest frequency of amplifier passband.

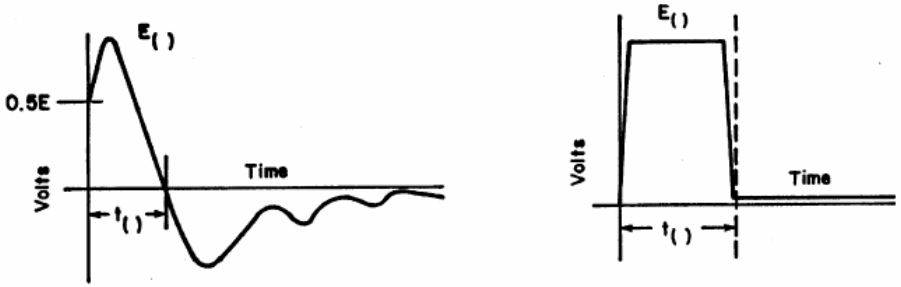
f_2 = Highest tunable frequency of receiver band in use or the highest frequency of amplifier passband.

W = Bandwidth between the 80 dB points of the receiver selectivity curve as defined in the test sample's technical requirements or the control plan.

Limits:

1. The limit at A is 80 dB above the input level required to produce the standard reference output. (This limit shall not be used for amplifiers)
2. The limit at B shall be set as follows:
   a. Receivers: 0 dBm applied directly to the receiver input terminals.
   b. Amplifiers: The limit shall be as specified in the test sample's technical requirement or control plan. If no limit is defined in the above documents, the 0 dBm value shall be used.

FIGURE 2-5. LIMIT FOR CSO4



NOTE: The test sample shall be subjected to the spike(s) with the waveform shown and with the specified voltage(s) and pulsewidth(s).

FIGURE 2-6. ACCEPTABLE WAVESHAPES FOR CSO6 AND RSO2

MIL-STD-461C

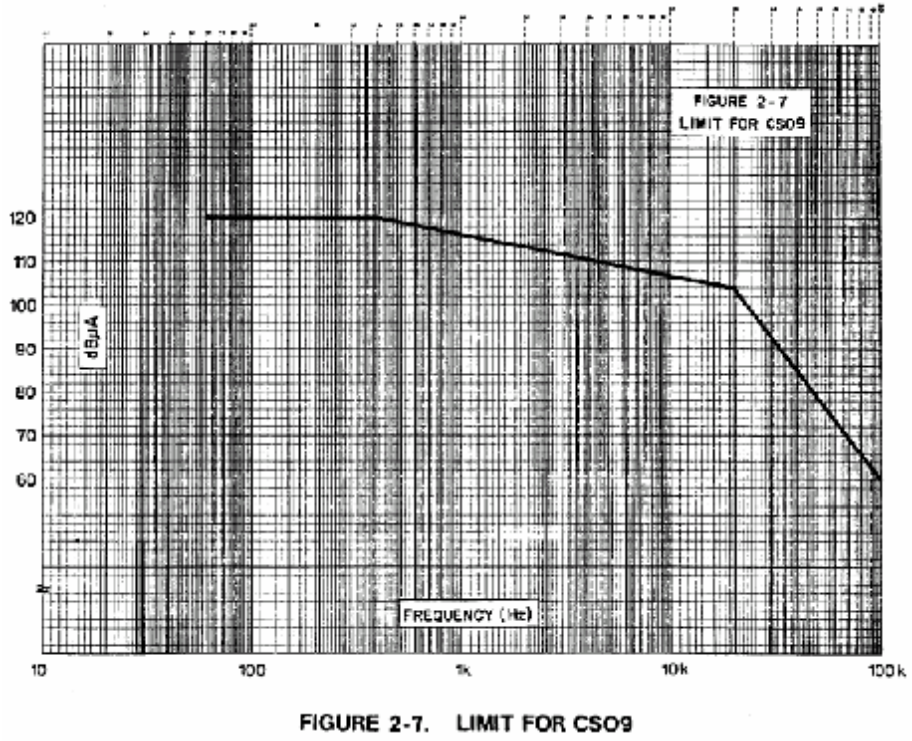


FIGURE 2-7. LIMIT FOR CS09

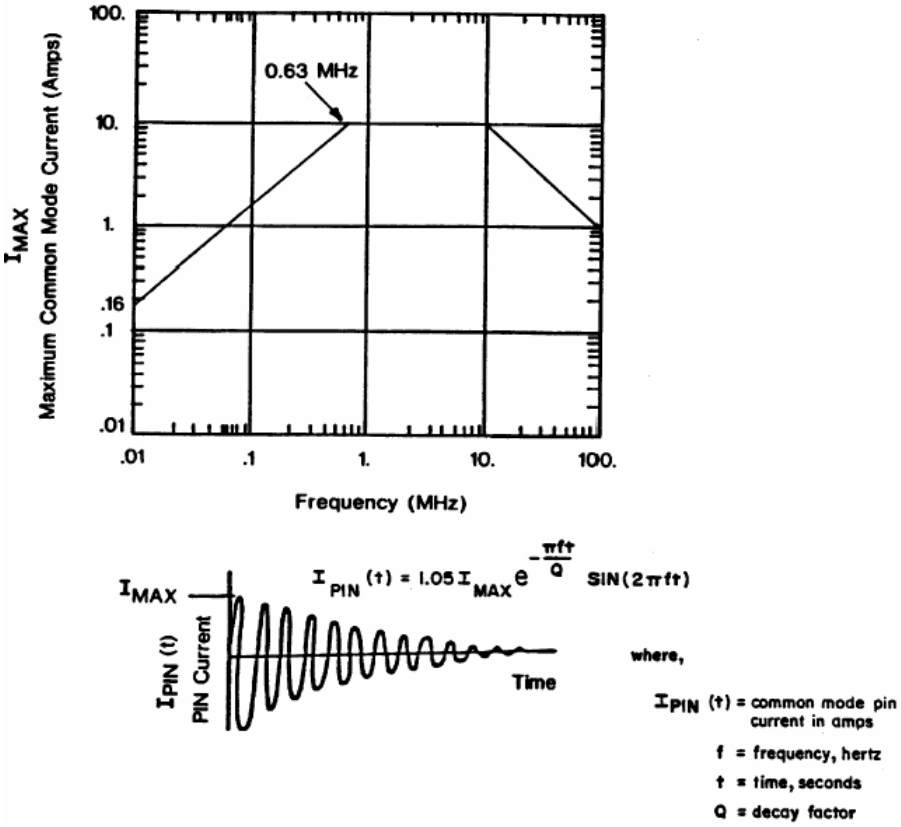


FIGURE 2-8. LIMIT FOR CS10

MIL-STD-461C

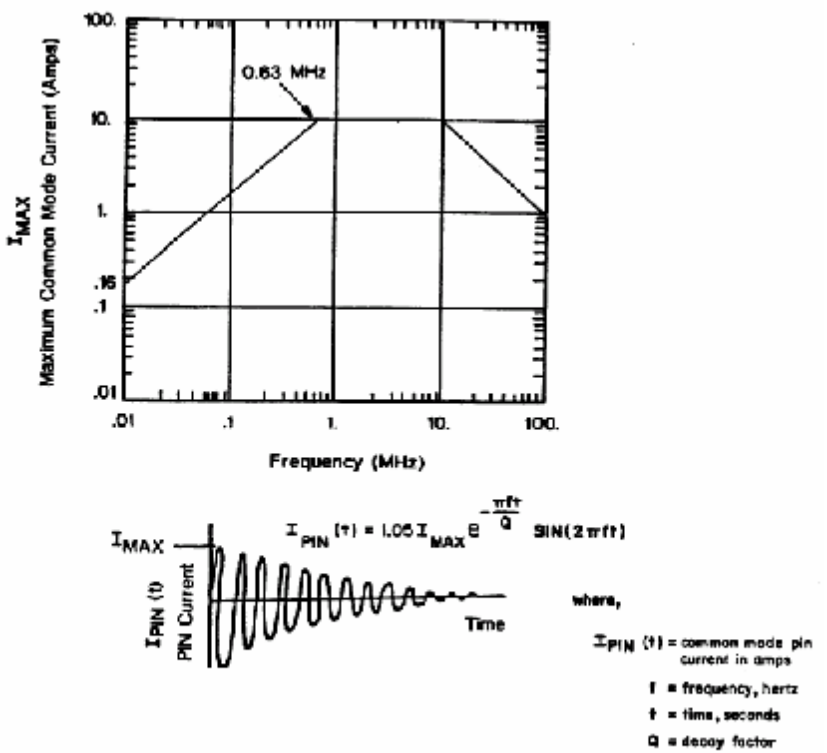


FIGURE 2-8. LIMIT FOR CS10

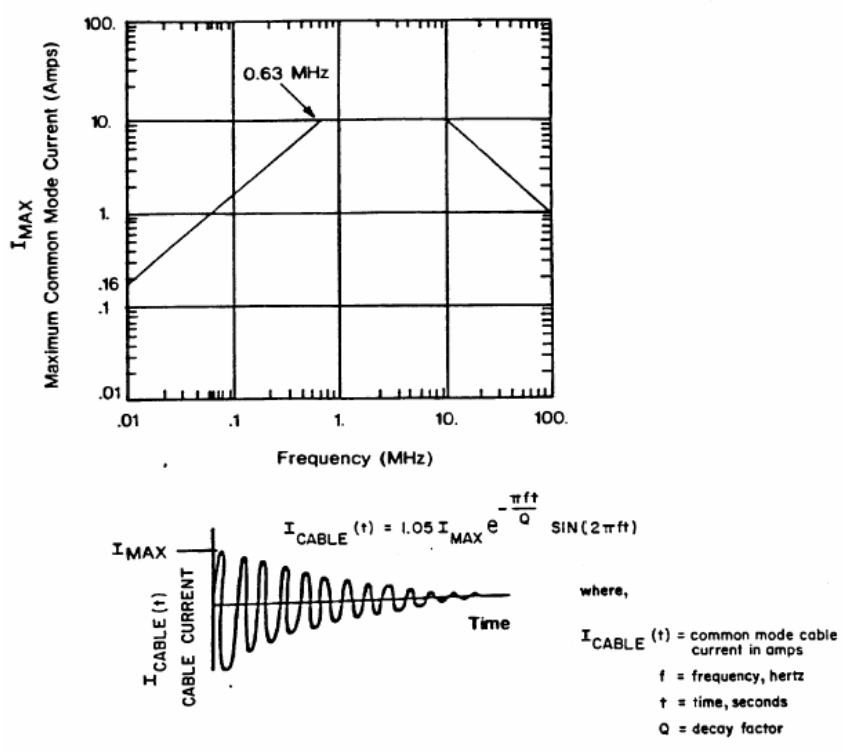


FIGURE 2-9. LIMIT FOR CS11

MIL-STD-461C

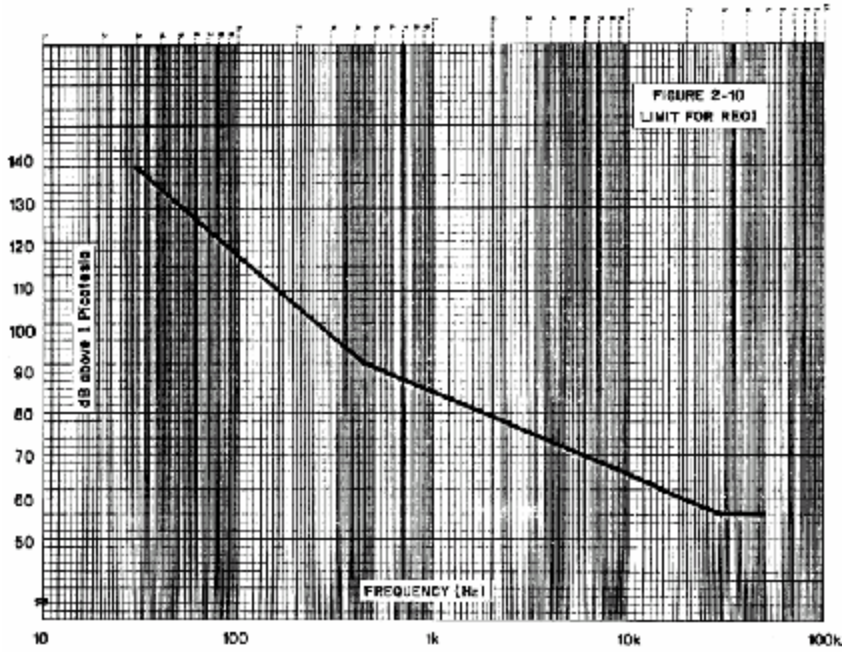


FIGURE 2-10. LIMIT FOR RE01

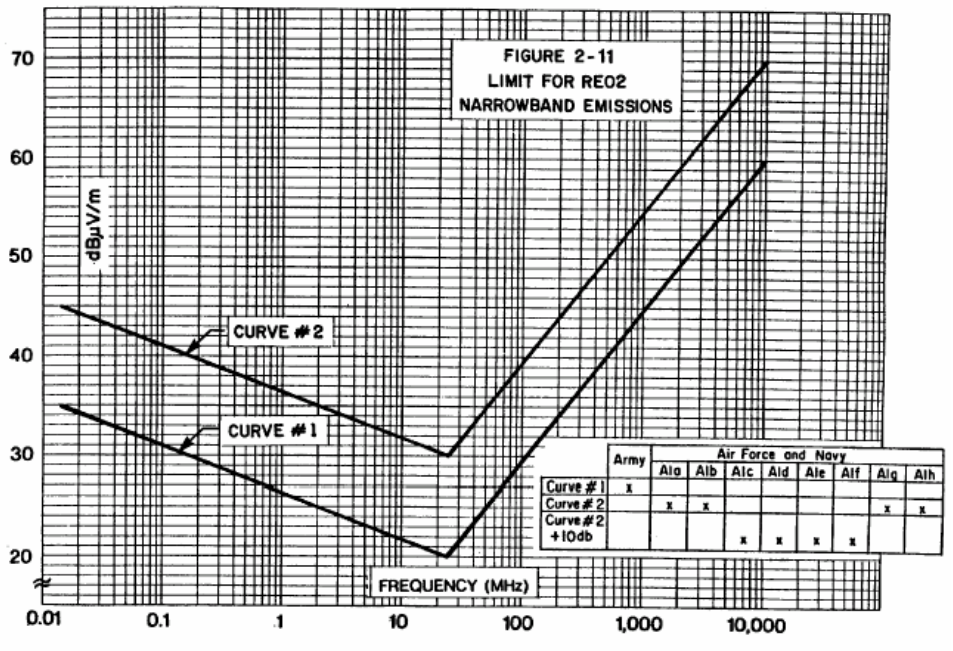


FIGURE 2-11. LIMIT FOR RE02 NARROWBAND EMISSIONS

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Condicionantes Mecánicos

Dimensiones y forma de la estructura o caja soporte

Material de fabricación

Determinar el sistema de fijación

Dimensión y posición de los puntos de fijaciones

Considerar requerimientos de vibración

Tener en cuenta la Rigidez Flexibilidad

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Condiciones Térmicas

Para el diseño del pcb es importante conocer el comportamiento térmico ⇒

-Determinar/calcular la disipación de los componentes mas significativos

-Determinar las resistencias térmicas al TRP (Thermal reference point)

-Conocer en su caso el rango de temperatura del soporte o estructura

-Realización de análisis térmico

-En función de los de los resultados

reposicionar componentes

búsqueda de caminos o vías de disipación

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Consideraciones Diseño PCB I

Para el diseño del PCB se tendrán en cuenta:

Encapsulados, creación o supervisión conforme a estándares

ejemplo MIL-PRF-55365/4 encapsulado CWR06

Posicionado

Tipo (digital analógico mixto)

Disipación

Generación de ruido o susceptibilidad al mismo

Diseño en función de las normativas existentes

ECSS (European Cooperation for Space Standardization)

ECSS-Q-70-10A (Qualification of printed circuit boards)

ECSS-Q-70-11 (Procurement of printed circuit boards)

CNES (Centre National D' Etudes Spatiales)

CNES/QFT/SP.0050 (Specification for Design of printed circuit boards)

CNES/QFT/SP.0117 reemplazada por ECSS-Q-70-10

CNES-QFT-SP 0119

Consideraciones Diseño PCB II

ESA (European Space Agency)

- ESA CNES-QFT-SP 0117 (Cualification & procurement of two-side PCB's)
- ESA CNES-QFT-SP 0119
- ESA PSS-01-710 Reemplazada por ECSS-Q-70-10

DSP (Defense Standardization Program)

- Mil-P-55110 (Printed Wiring Board, Rigid, General Specification For)
- Mil-P-50884 (Printed Wiring, Flexible and Rigid-Flex (w/Amendment 2))

IPC (Institute for Printed Circuits), (Institute of Interconnecting and Packaging Electronic Circuits)
(IPC ASSOCIATION CONNECTING ELECTRONICS INDUSTRIES) www.ipc.org

- IPC-2221 (Generic Standard on Printed Board Design)
- IPC-6012A (Qualification and Performance Specification for Rigid Printed Boards)
- IPC-6013 (Qualification and Performance Specification for Flexible Printed Boards)
- IPC-7721 (Repair & Modification of PCB's & Electronics Assemblies)

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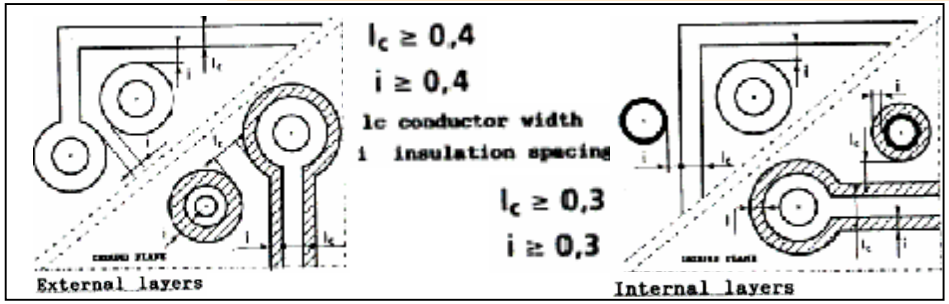
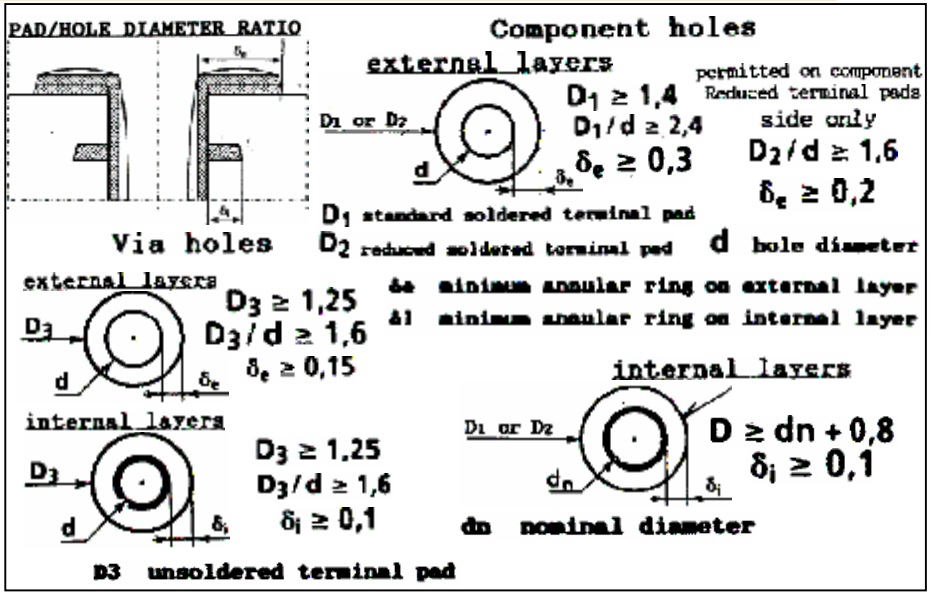
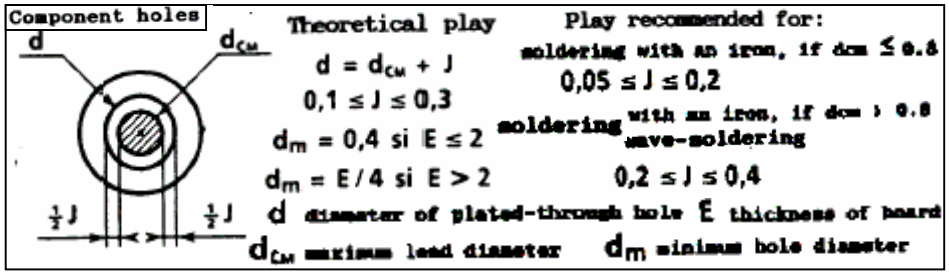
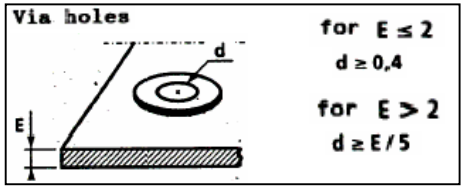
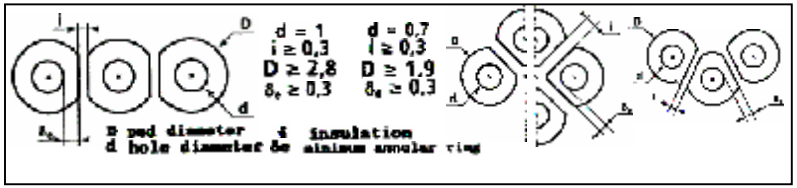
CNES/QFT/SP.0050 – 2A

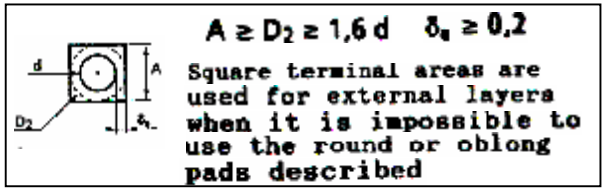


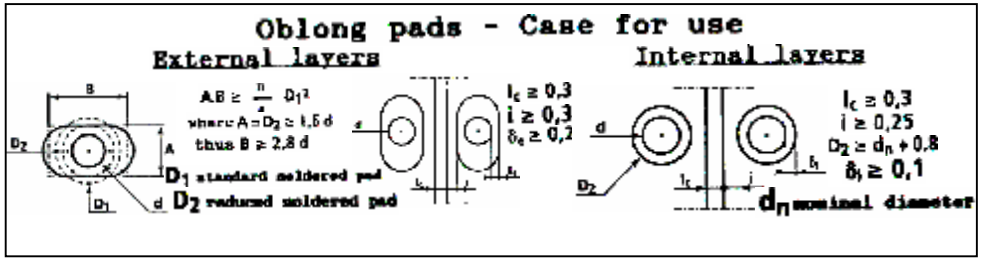


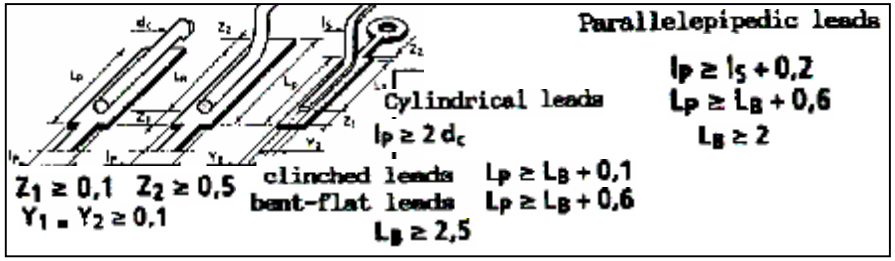












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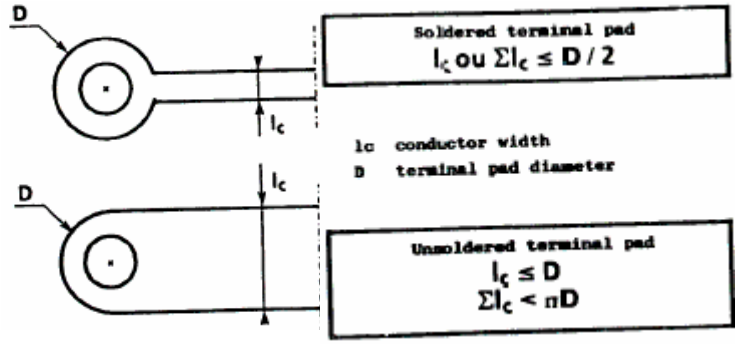
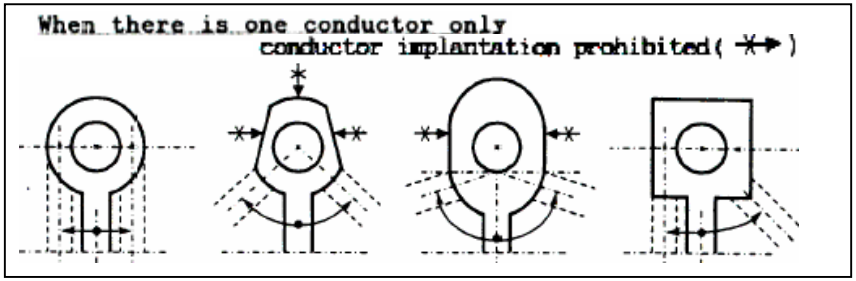
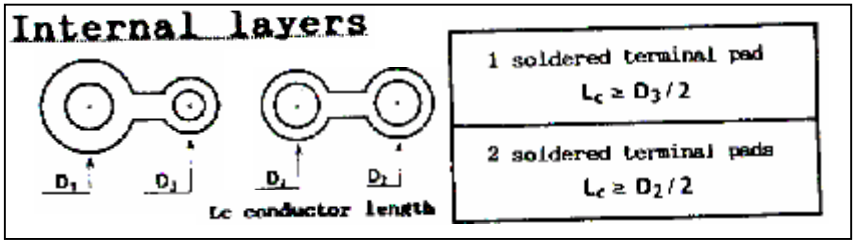
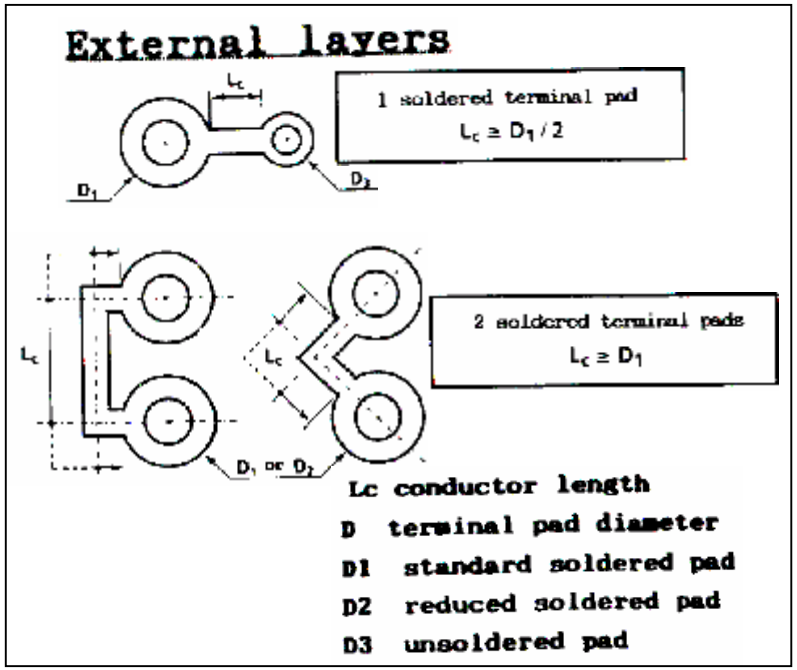
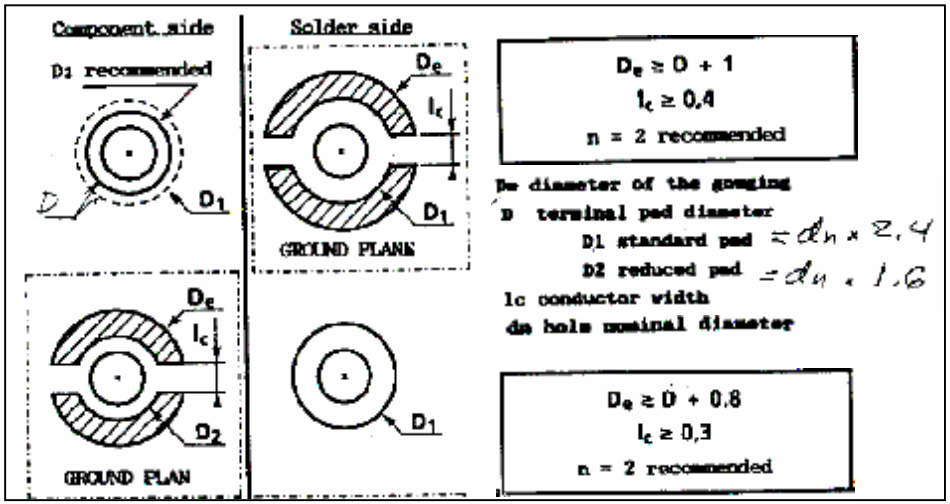






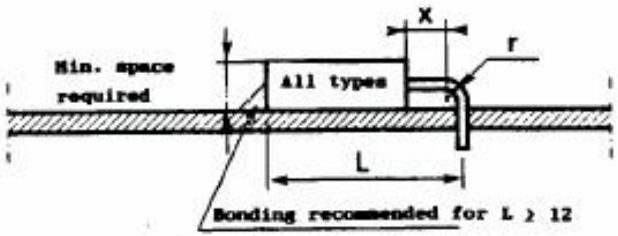




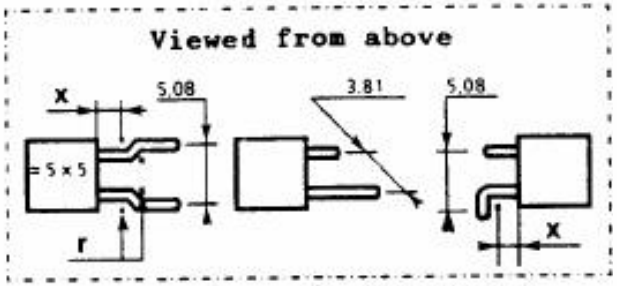
CNES/QFT/SP.0050 – 2A

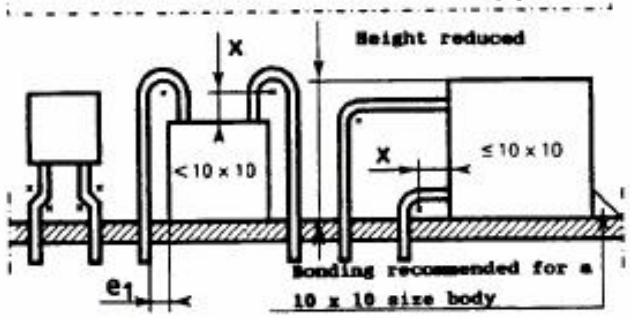
Special case

a) Parallelepipedic packages



- Changing lead pitch -





$x \geq 1,6$

$r \geq d_c$ si $d_c \leq 0,6$

$r \geq 2d_c$ si $d_c > 0,6$

$3 \leq h_2 \leq 5$

$e_1 > 0$

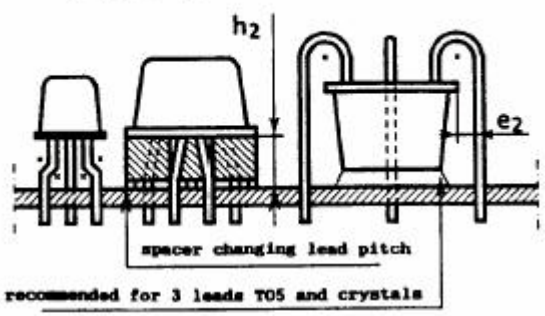
body or leads insulated

$e_2 \geq 1$

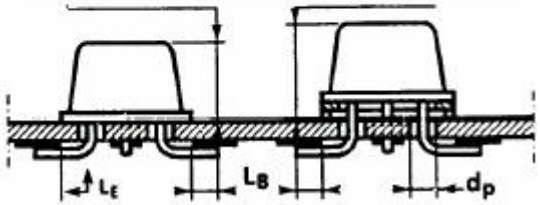
body and leads non-insulated

dc diameter of the lead
x distance before bend
r radius of flexion
b distance between the body of the component and the board
e spacing
Dc diameter of the component

b) Round packages



Space required reduced, with or without spacer



$L_B \geq 2,5$

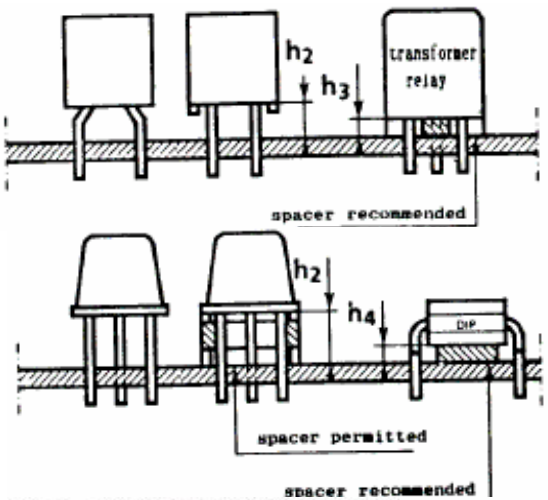
$L_E \geq 3$

$d_p \geq d_c + 0,2$

LB length of lead to be soldered
LE length of lead before soldering
dp diameter of non-plated through holes

CNES/QFT/SP.0050 – 2A

General case

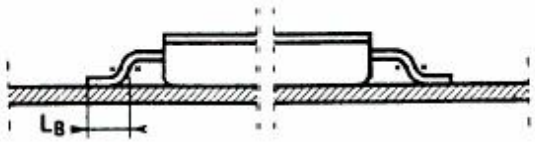


$3 \leq h_2 \leq 5$
$h_3 \geq 2$

h distance between the body of the component and the board

$h_4 \geq 2$ recommended depending on board thickness

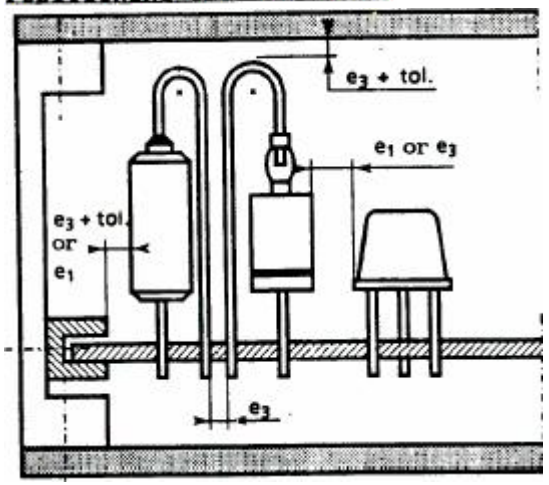
3.4 FLAT-PACK COMPONENTS



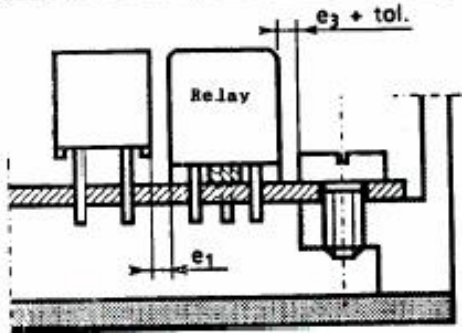
$L_B \geq 2$

L_B length of lead to be soldered

POSITIONING OF COMPONENTS



$e_1 > 0$
one element is insulated
$e_3 > 0,5$
elements non-insulated



C

C

C

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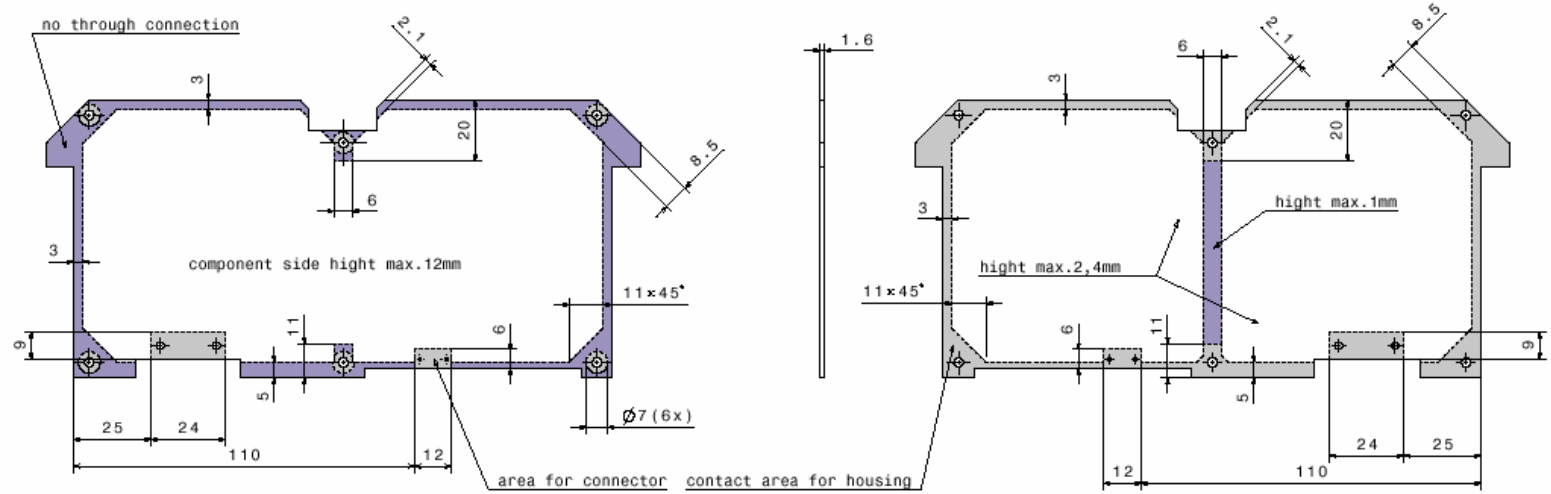
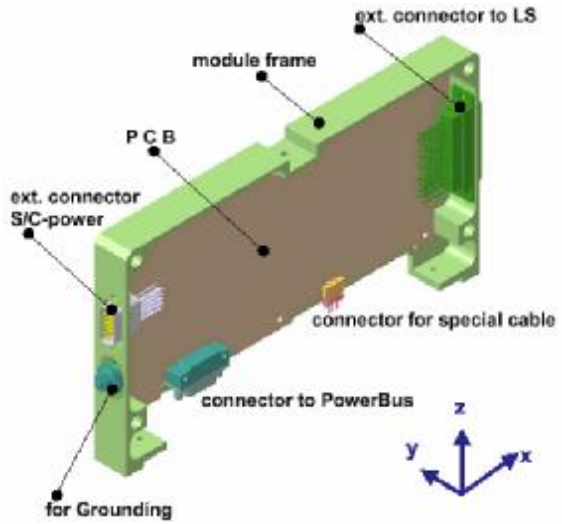
Dimensiones mecánicas proyecto II





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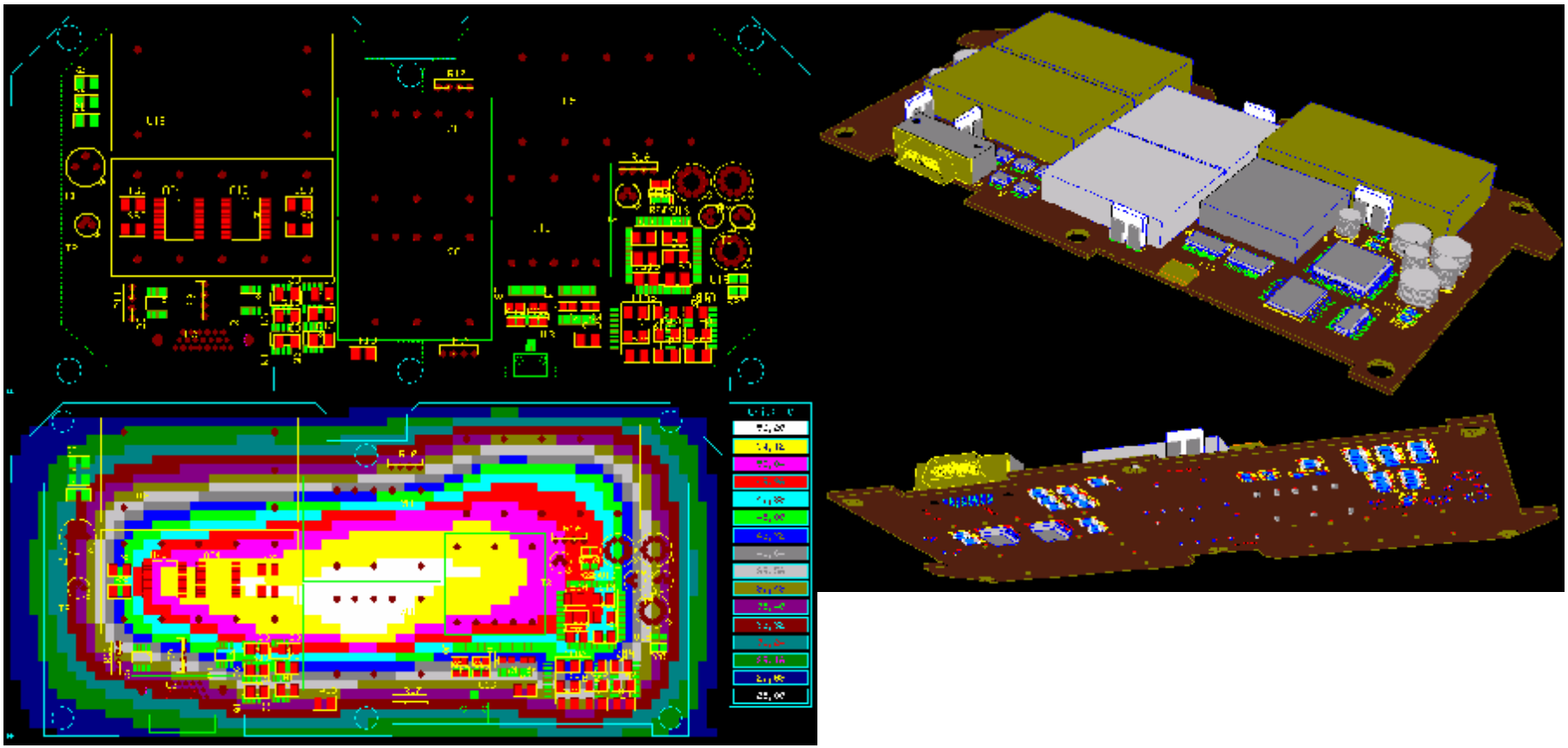
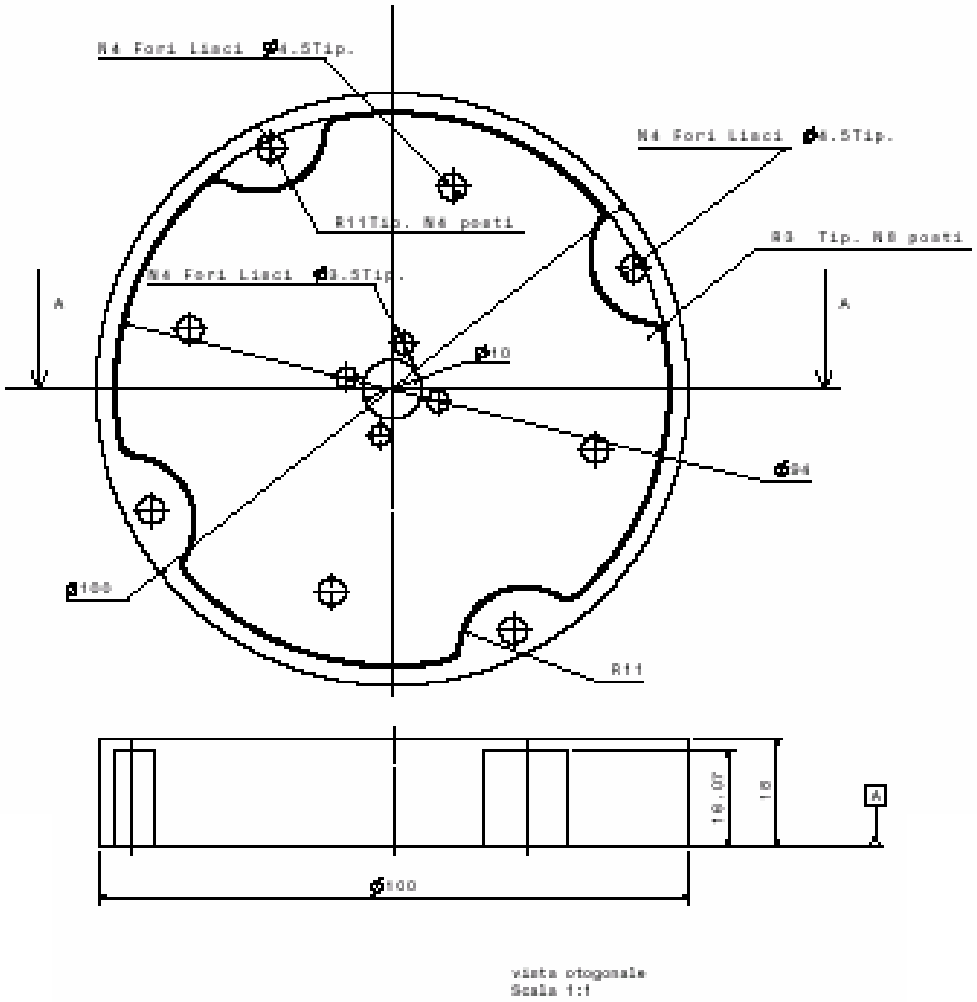
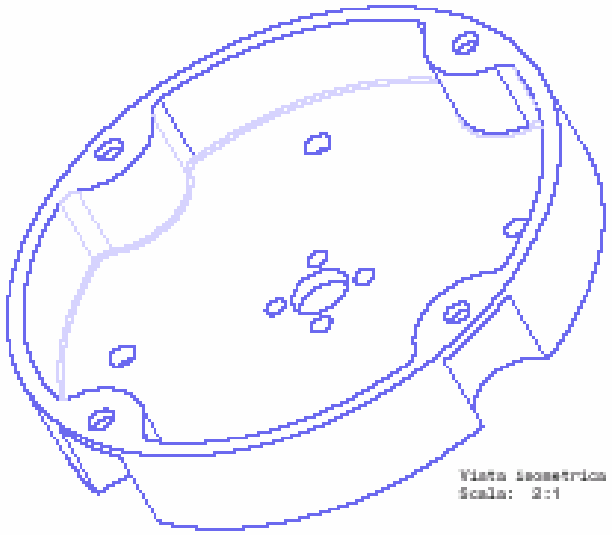
Estudio PCP Proyecto II



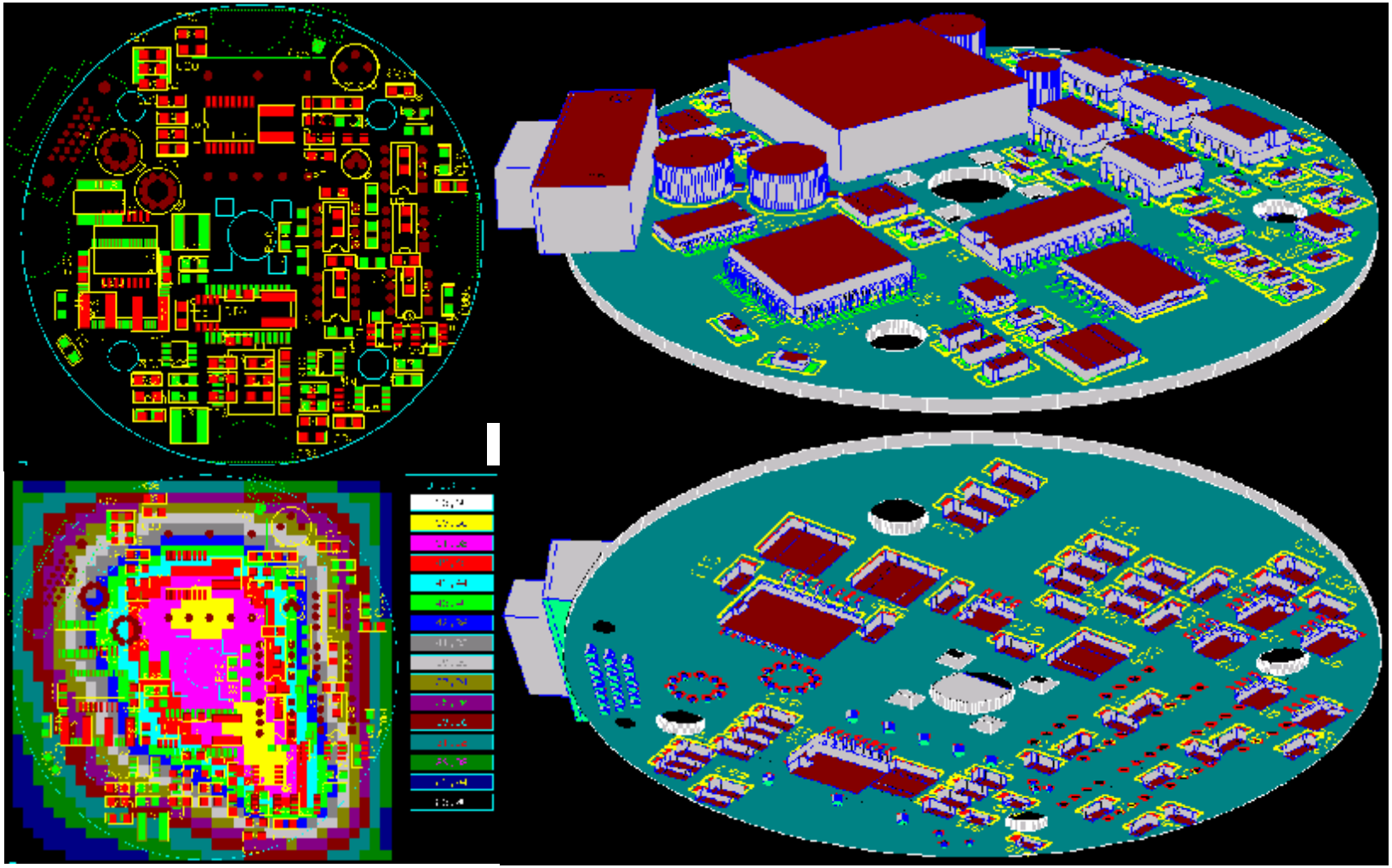
Dimensiones mecánicas proyecto III





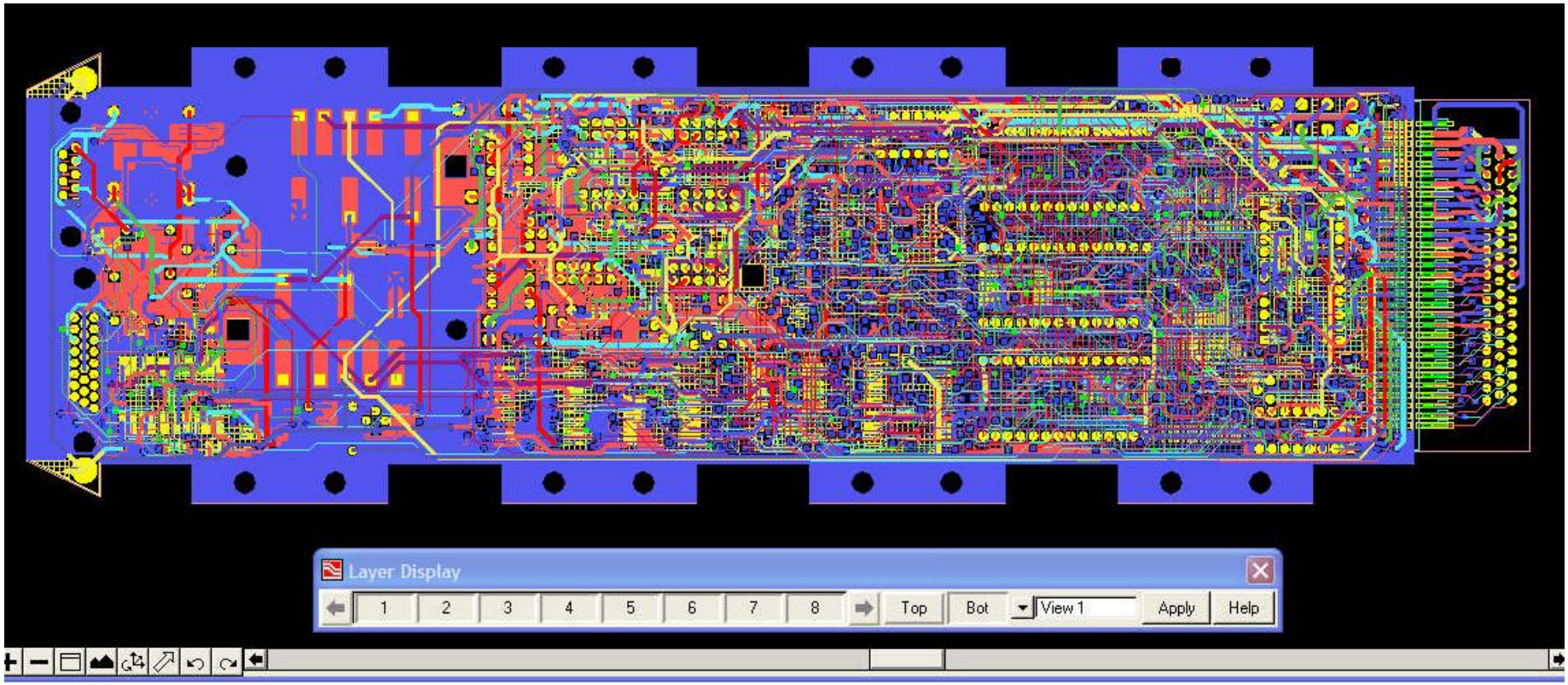
PADS PCB Design Solutions

Estudio PCP Proyecto III

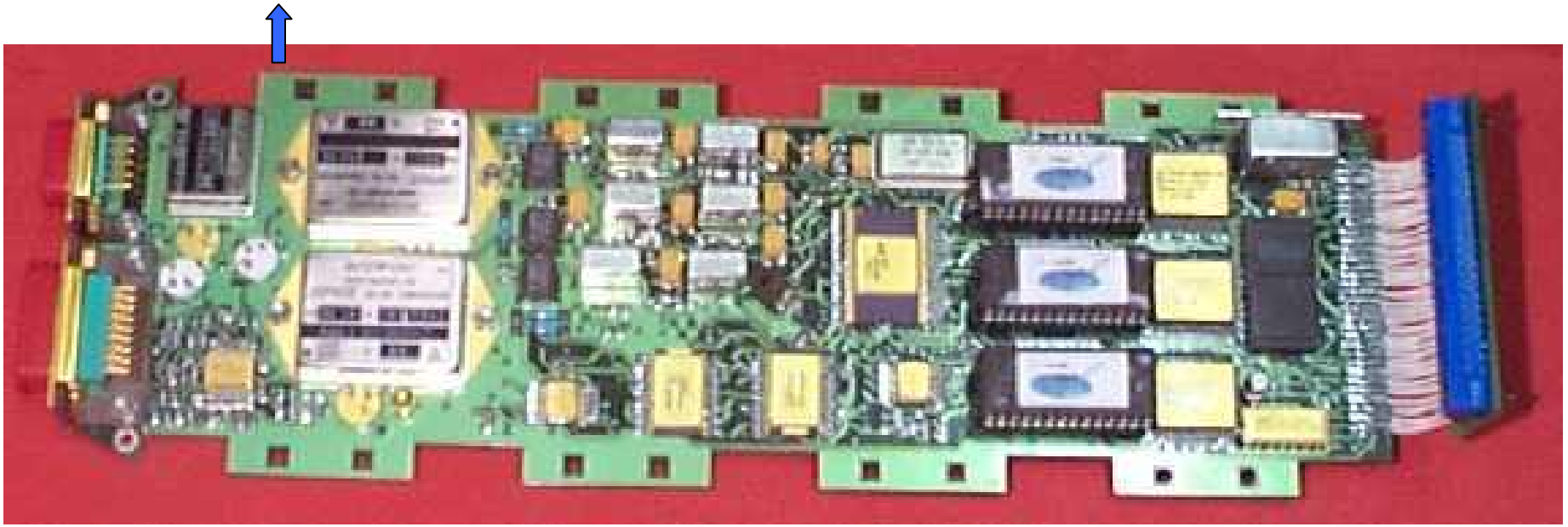


PADS PCB Design Solutions

PCB CPU/PS EQM

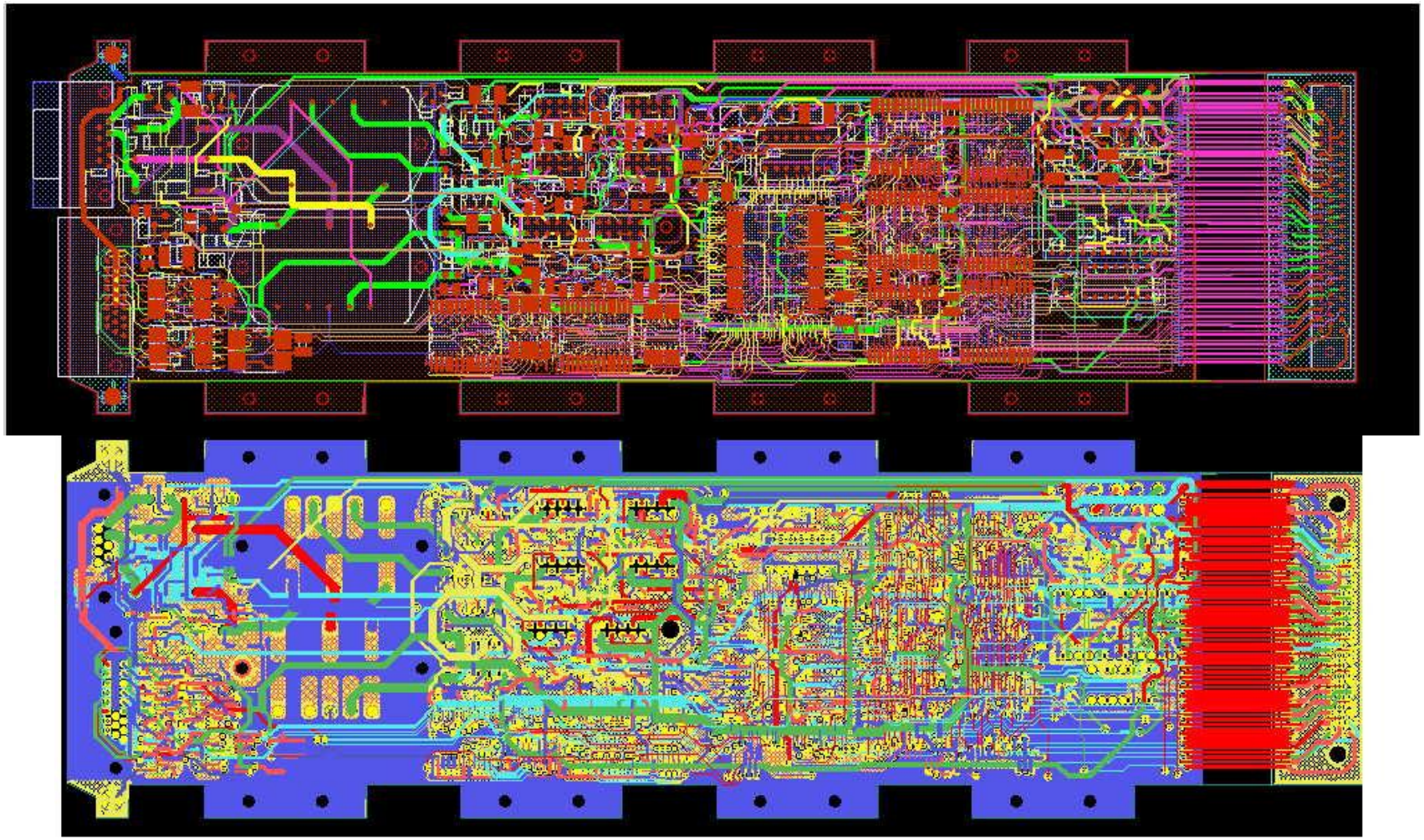


CPU/PS EQM

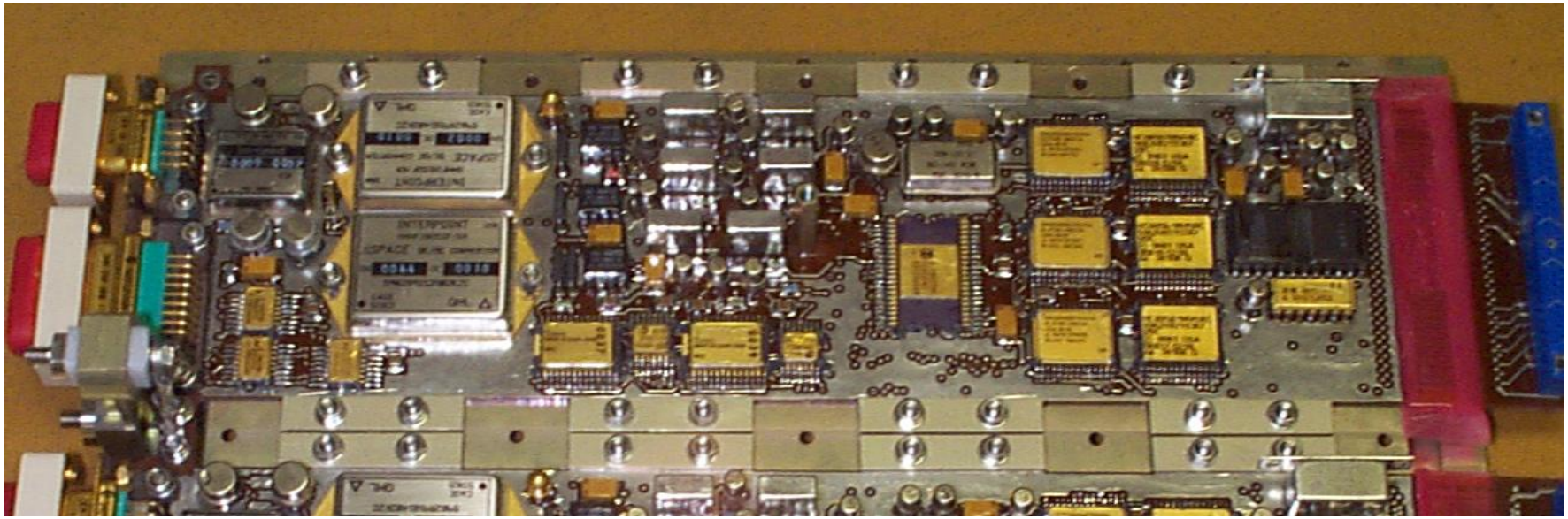


PADS
PCB Design Solutions

PCB CPU/PS QM-FS

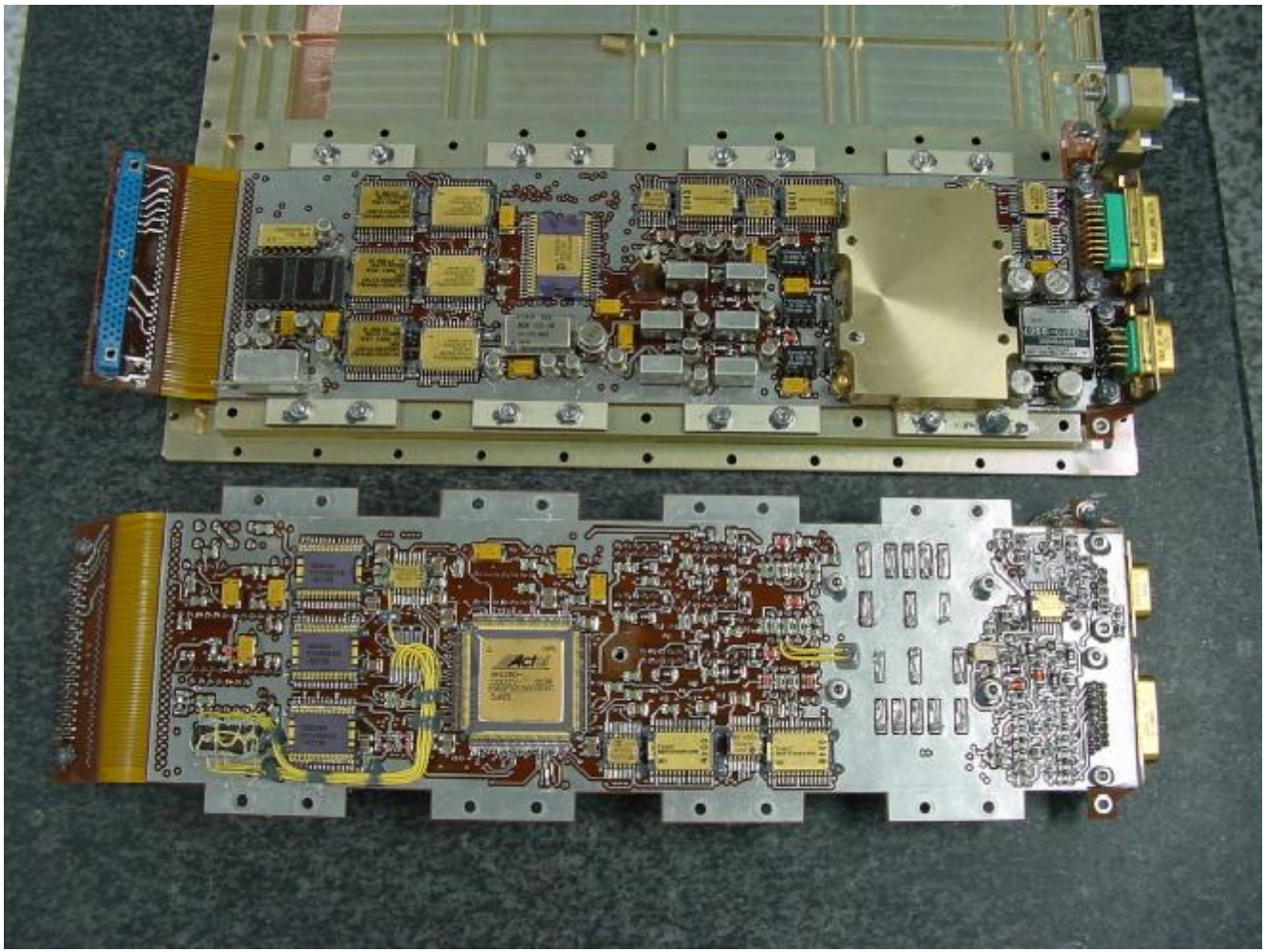


CPU/PS FM



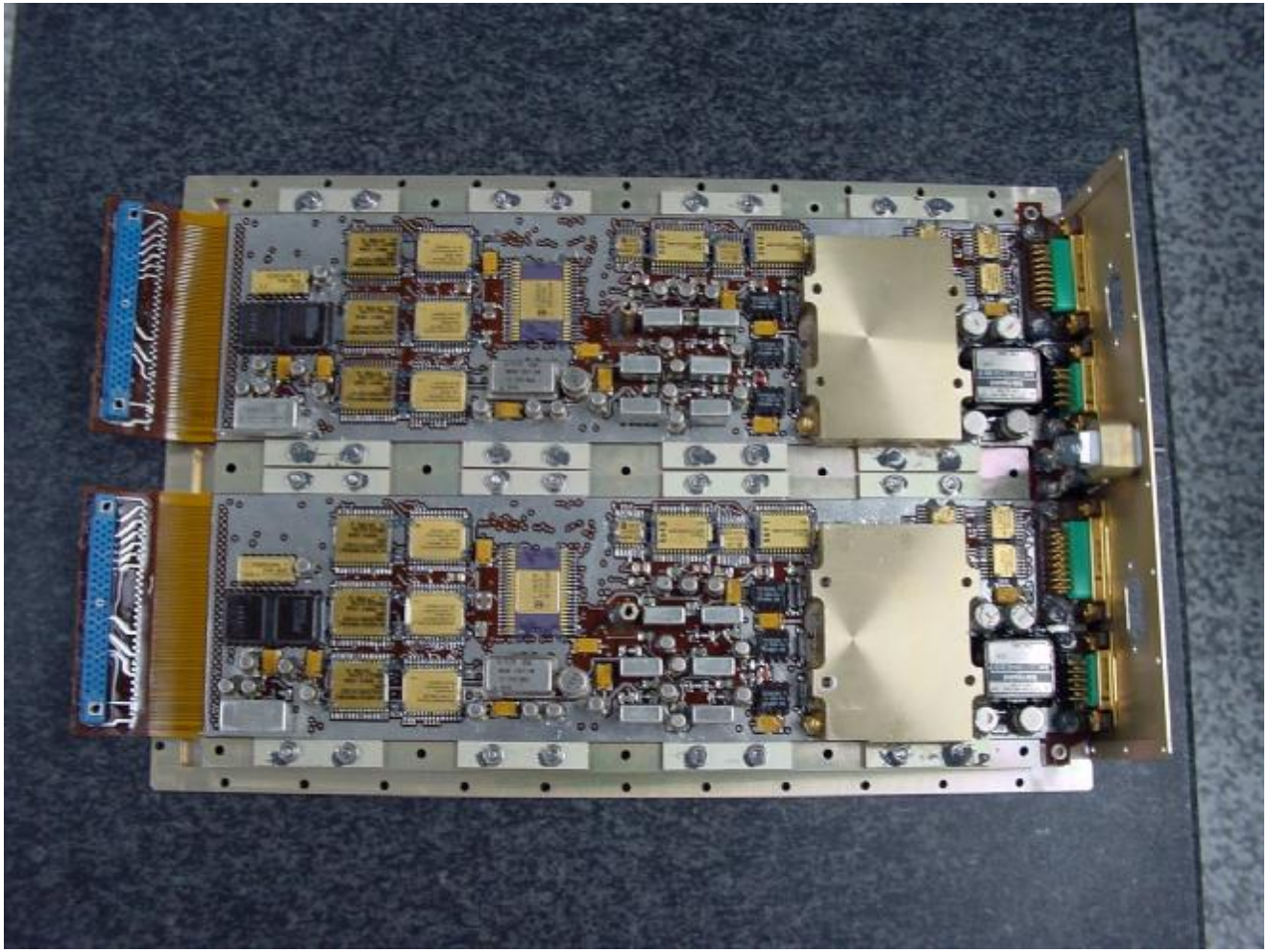
PADS PCB Design Solutions

CPU/PS's Main & Redundant FM



PADS PCB Design Solutions

CPU/PS's Main & Redundant FM



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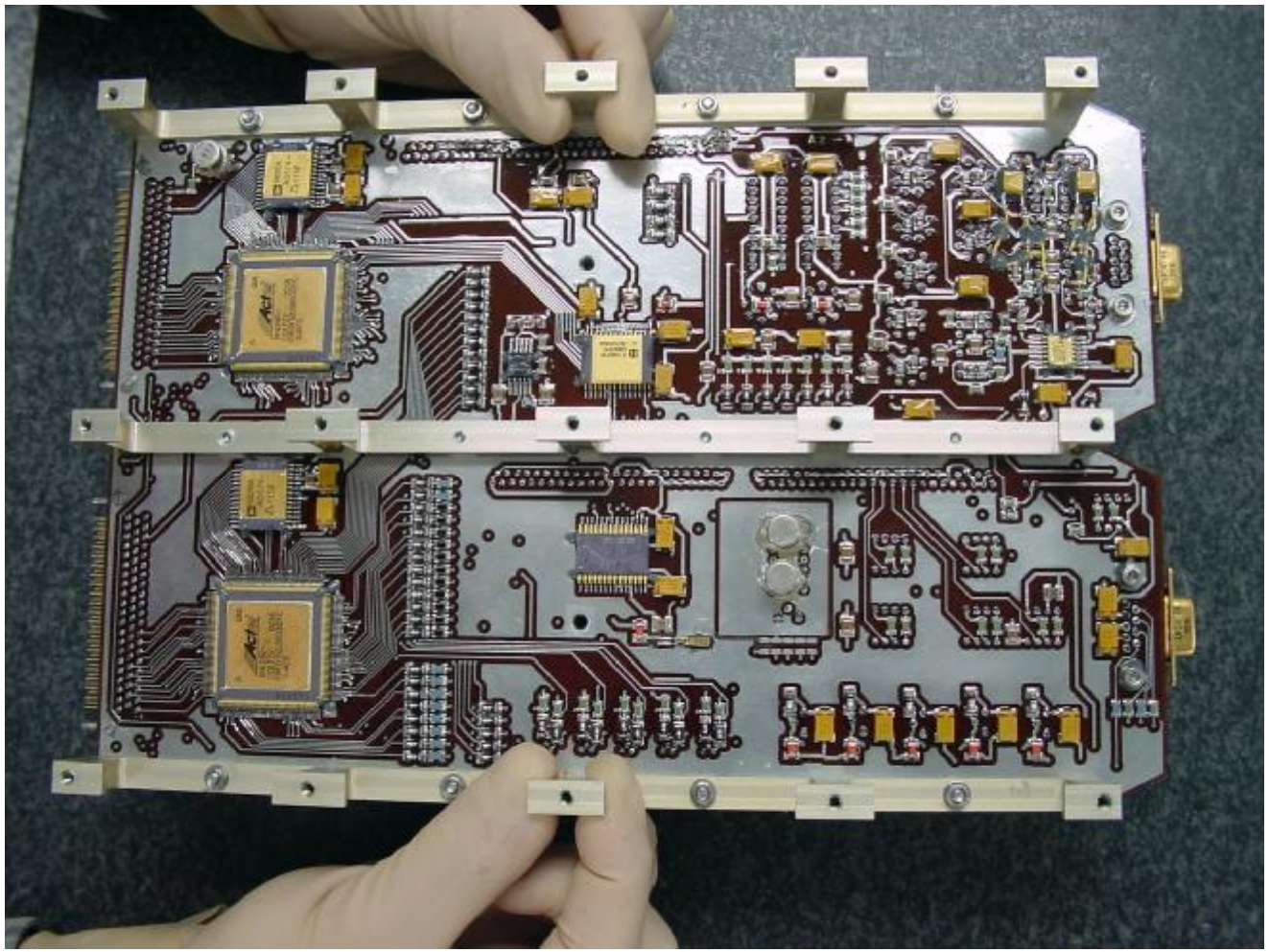
Analógica FM



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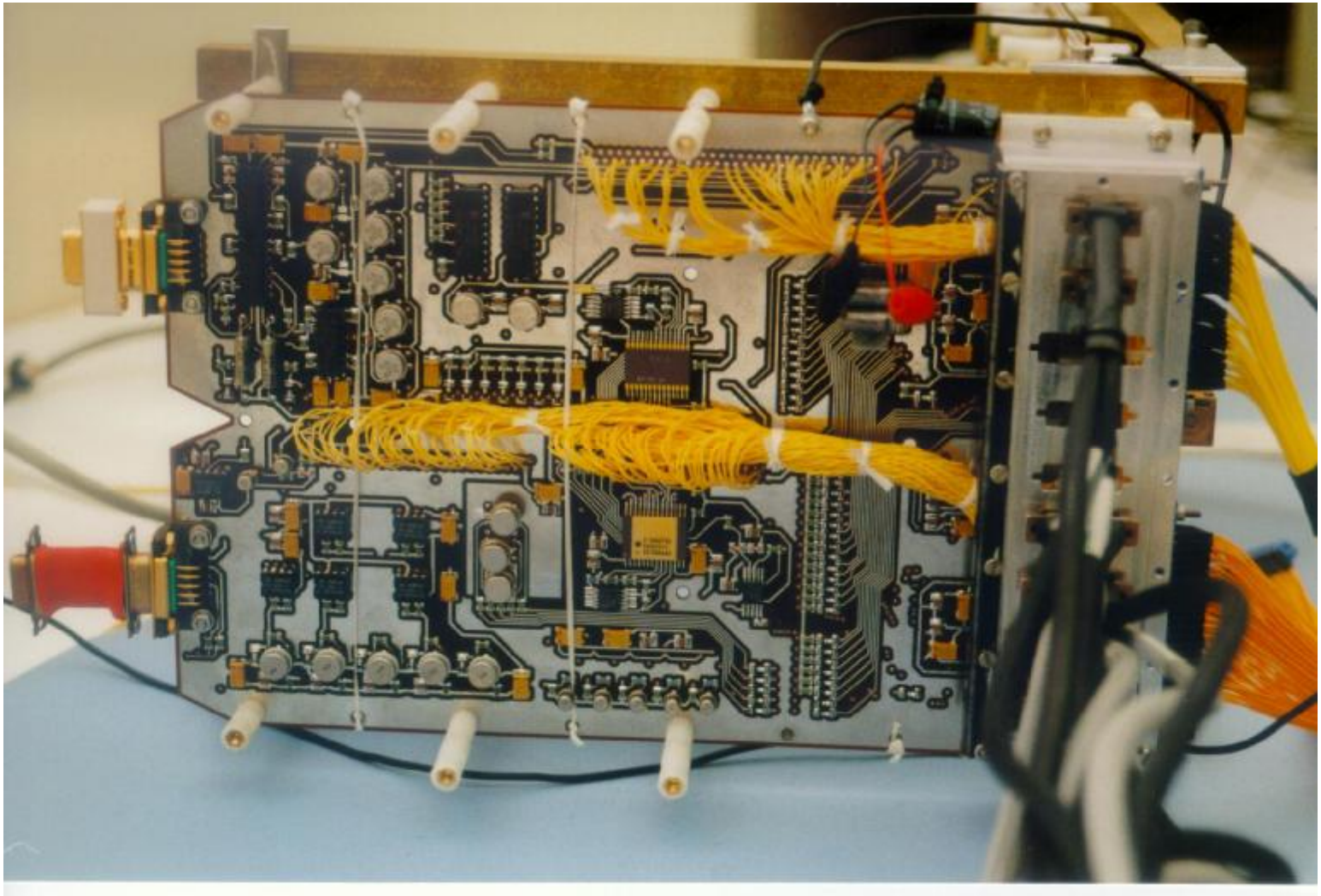
PCB Design Solutions

Analógica FM



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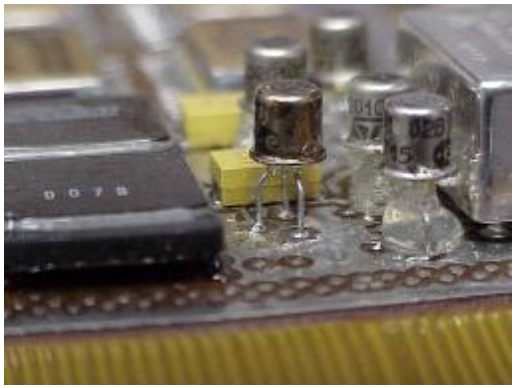
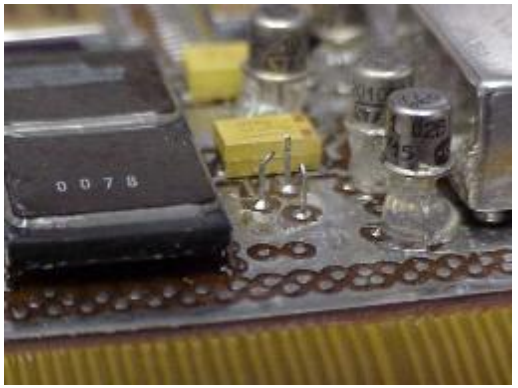
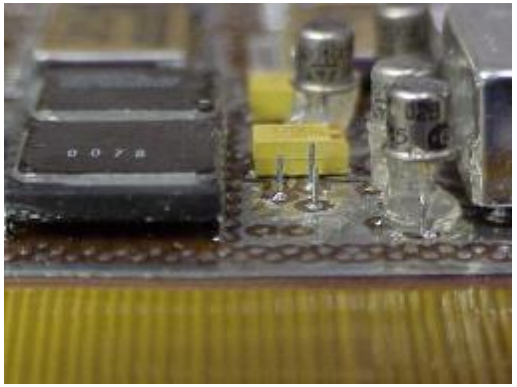
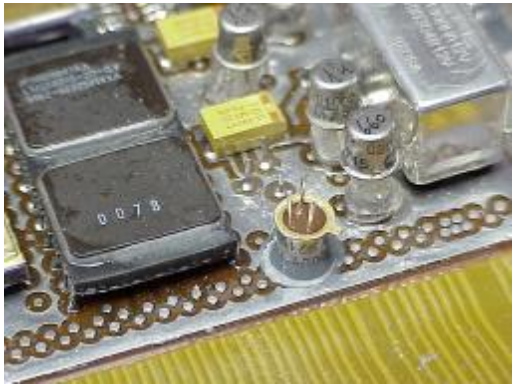
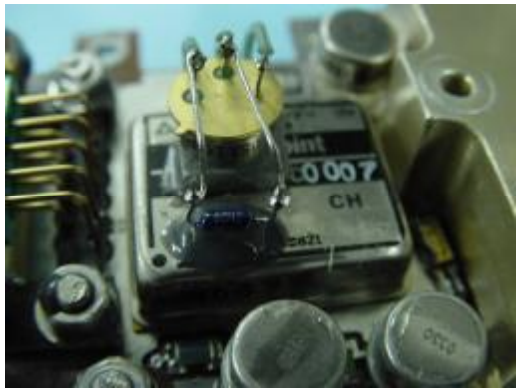
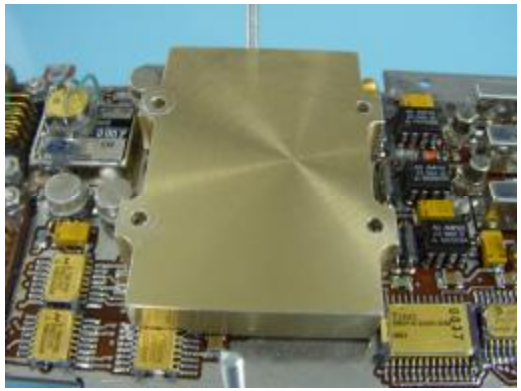
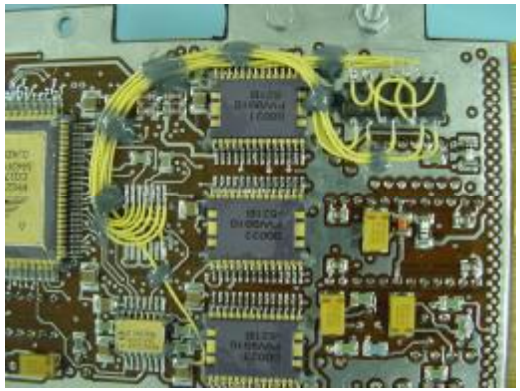
Reparación Cualificada


Ultimas correcciones







Muchas GRACIAS